	DRAWI	NG NO.	REV.		SHEET		SCALE	SIZE	Ē				
	1019-	-1618	V	1	OF	7	NTS	A					
		14							-	REVISIONS			
REV.	ECO NO.					Γ	DESCR	IPTIC	ON	OF UPDATE	AP	PROVED	DATE
-	RLSD	N/A						D. MILL	.ER	02/87			
A	1481	Per ECO									D. MILL	.ER	08/88
В	2054	Per ECO									D. MILL	.ER	12/90
С	2203	Per ECO							3.		C. HEIS	SELMAN	03/91
D	3183	Per ECO									C. HEIS	SELMAN	12/08/92
E	5227	Per ECO									C. HEIS	SELMAN	07/10/96
F	6716	Per ECO						C. HEIS	SELMAN	04/16/98			
G	9581	Per ECO									C. HEIS	SELMAN	12/27/01
Н	10824	Per ECO									C. HEIS	SELMAN	03/19/03
J	11715	Per ECO									C. HEIS	SELMAN	07/11/04
K	13372	Per ECO									C. HEIS	SELMAN	03/23/06
L	16865	Add 4.1.3 flow c	Jown to	sub	tier						C. HEIS	SELMAN	01/21/10
M	20757	Add 4.1.10 Req	uiremer	nts fo	or reco	ord r	etentior	n			C. HEIS	SELMAN	01/03/14
Ν	176066	Tie in Anaren D in 81000.	oc. #81	000,	gene	ral c	larificat	ion, r	rem	ove redundant information now located	B. HAH	N	02/27/15
P	183404	Add gel pak opt	ion, ren	nove	test s	amp	ole deliv	/ery f	for	Condition E	B. HAH	N	02/22/16
R	197543	Add "Space Dat	ta Pack	age"	' to "Te	est c	lata"				B. HAH	N	07/27/17
Т	205458	Add waffle pack	specifi	icatic	ons						B./HAH	N	06/06/18
U	209822	Add packaging	requirer	men	ts and	upd	ate doo	cume	ent		L QOU	GLA9	09/10/18
V	210539	Add "NO STAC	K" requ	irem	ent to	pac	kaging				A	- VAV	10/19/19
													11

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DO NOT SCALE DRAWING	APPROVALS		Anaren°		DISTRIBUTION DATE			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE	J. VANDEUSEN	10/02/18						
FRACTIONS DECIMALS ANGLE ± - ± - ± - ± -	M. BAFTING CHECK	10.12.18	FOR	ECIFI	CAT	ION		
MATERIAL N/A	ENGINEERING CHECK	10-15-18	MICROCIRCUIT / SEMICONDUCTOR					
FINISH N/A	CUALITY ASSURANCE	10-11-18	drawing no. 1019-1618	^{REV.}	1	SHEET OF	7	DEPARTMENT

DRAWING NO.	REV.	SHEET	SCALE	SIZE
1019-1618	V	2 OF 7	NTS	Α

1.0 <u>PURPOSE:</u>

The purpose of this document is to define the supplier requirements of all procured microcircuit elements (Integrated Circuits) and semiconductor elements (diodes, transistor, etc.) used in devices. This document is used in conjunction with Anaren Document #81000.

2.0 <u>APPLICATION:</u>

This procedure shall apply to all microcircuit elements and semiconductors as follows:

- 2.1 <u>Condition A</u> Elements to be used in compliance with MIL-PRF-38534 Class H devices. Element evaluation shall be performed IAW MIL-PRF-38534 Class H and data provided with delivery. Note 1.
- 2.2 <u>Condition B</u> Elements intended to be used in full compliance with MIL-PRF-38534 Class H but element evaluation will be the responsibility of the user. Supplier/Mfg is responsible for 100% visual and electrical. Note 1.
- 2.3 <u>Condition C</u> Elements to be used on devices which do not impose MIL-PRF-38534 element evaluation.
- 2.4 <u>Condition D</u> Elements to be used in compliance with MIL-PRF-38534 Class K devices. Element evaluation shall be performed IAW MIL-PRF-38534 Class K and data provided with delivery. Note 2.
- **2.5** <u>Condition E</u> Elements tested IAW the element drawing. When specified on the PO, 12 die shall be packaged and shipped to the user for Radiation Testing. Note 2.

<u>NOTE 1</u> For Class H devices, element evaluation testing is not required for JANHC or JANKC discrete semiconductor which have been tested in accordance with MIL-PRF-19500, or if the microcircuit die are MIL-PRF-38535 Class Q or V qualified. (Class Q is equivalent to Hybrid Class H and Class V is equivalent to Hybrid Class K)

<u>NOTE 2</u> For Class K devices, element evaluation testing is not required for JANKC discrete semiconductor which have been tested in accordance with MIL-PRF-19500, or if the microcircuit die are MIL-PRF-38535 Class V qualified (Class V is equivalent to Hybrid Class K)

3.0 **DEFINITIONS:**

- 3.1 <u>Element</u> A constituent of the hybrid microcircuit that contributes directly to its operation. The element shall be coated, except bonding pads, with an approved transparent glass to a minimum thickness of 200 nm of Si_3N_4 or equivalent.
- 3.2 <u>Microcircuit</u> A small active circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on one or more substrates to perform an electronic circuit function. The microcircuit shall be coated with a transparent glass or other approved coating to a minimum thickness of 600nm for SiO_2 and 200nm for Si_3N_4 and shall cover all conductors except bonding pads.

Internal thin film conductors on a substrate (metallization stripes, contact areas, bonding interfaces, etc.) shall be designed so that no properly fabricated conductor shall experience in normal operation (at worst case specified operating conditions), a current density in excess of the maximum allowable value shown below for the applicable conductor material:

Conductor Material	Maximum Allowable Current Density
Aluminum (99.99 percent pure or doped) without glassivation.	$2 \text{ X} 10^5 \text{ A/cm}^2$
Aluminum (99.99 percent pure or doped) glassivated.	$5 \text{ X} 10^5 \text{ A/cm}^2$
Gold	$6 \text{ X } 10^5 \text{ A/cm}^2$
All other (unless otherwise specified)	$2 \text{ X} 10^5 \text{ A/cm}^2$

The current density shall be calculated at the point of maximum current density (ie. greatest current per unit cross section) for the specified device type and schematic or configuration.

PROCUREMENT SPECIFICATION FOR	DRAWING NO.	REV.	SHEET		DEPARTMENT
MICROCIRCUIT / SEMICONDUCTOR	1019-1618	V	2 OF	7	

DRAWING NO.	REV.	SHEET	SCALE S	IZE
1019-1618	V	3 OF 7	NTS	Α

- **3.3** <u>Wafer Lot</u> Wafer lots consist of microcircuit and semiconductor wafers formed into lots at the start of wafer fabrication for homogeneous processing as a group. Each lot is assigned a unique identifier or code to provide traceability and maintain lot integrity throughout the fabrication process. Wafer lot processing as a homogeneous group is accomplished by any of the following procedures, providing process schedules and controls are sufficiently maintained, to assure identical processing in accordance with process instructions of all wafers in the lot:
 - a. Batch processing of all wafers in the wafer lot through the same machine process steps simultaneously.
 - b. Continuous or sequential processing (wafer by wafer or batch portions of wafer lot) of all wafers through the same machine or process steps.
 - c. Parallel processing of portions of the wafer lot through multiple machines or process stations on the same certified line, provided statistical quality control (SQC) assures and demonstrates correlation between stations and separately processed portions of the wafer lot.
- **3.4** <u>**Production Lot**</u> A production lot consists of a device type manufactured from the same basic raw materials on the same production line, processed under the same manufacturing techniques and controls using the same type of equipment. Each lot shall be assigned a unique identification that provides traceability to all processing steps.
- **3.5** <u>Inspection Lot</u> An inspection lot shall consist of microcircuits/semiconductors of a single circuit type submitted at one time for inspection to determine compliance with the applicable requirements and acceptable criteria.
- **3.6** <u>Element Evaluation</u> As applicable to this specification shall consist of Microcircuit/Semiconductor die evaluated IAW MIL-PRF-38534.
- 3.7 <u>Environmentally Controlled Area</u> An area which exhibits the following conditions:
 - **3.7.1** Temperature shall be $25^{\circ}C (+3/-5^{\circ}C)$
 - 3.7.2 Class 8 per ISO 14644-1, -2 or Class 100,000 per MIL-STD-209
 - **3.7.3** Humidity RH 30 to 65%
 - **3.7.4** Positive Pressure .01" water column or greater
 - **3.7.5** Element Storage shall be in a nitrogen atmosphere dry box.

4.0 **REQUIREMENTS:**

4.1 General:

- **4.1.1** All material and processes used by die processor will be suitable for polymeric adhesive, soldering and/or eutectic die mounting. As applicable to the element design, pad metallization shall be suitable for thermosonic, ultrasonic and/or thermo compression bonding of gold or aluminum wire and shall be capable of withstanding a pull test as specified per MIL-STD-883, Method 2011.
- **4.1.2** All electrical test (100%) and visual inspection (100%) may be done at the wafer level provided all rejects are identified and removed from the lot when dice are separated from the wafer.

4.2 <u>Packaging Requirements</u>:

4.2.1 <u>Packaging</u>:

Refer to element packaging Table 1.

Elements shall be packaged to prevent damage during shipment and for automated assembly.

4.2.2 <u>Package Marking</u>:

The element part number, manufacturer's name, manufacturer's lot number and quantity shall appear on each waffle tray/gel pack. All samples and test data shall be identified by its device type, manufacturer's name and manufacturer's lot number. Markings shall be sufficient for inspection lot traceability.

4.2.3 <u>Certificate of Compliance</u>:

As defined in document #81000.

PROCUREMENT SPECIFICATION FOR	DRAWING NO.	REV.		SHEET		DEPARTMENT
MICROCIRCUIT / SEMICONDUCTOR	1019-1618	V	3	OF	7	

	0.	REV.	SI		SCALE	SIZE	E								
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Element	Trues				cinent	, 1 at	Kaging K	Deeleesi	$a \sim D_{a}$	<u></u>	4				
Semiconductor elements (transistor and diode dice)		2" coi wi - c c c c c t 1 1 c c c c c c c i t 1 1 c c c i v i i c c i v i c c i v i c c i c c c c	 2" x 2" black conductive waffle tray with: carrier well must be deep enough so that the die surface is below the top plane of the waffle tray protective sheet or pad secure lid (hinge or clamp) 					Packagi	<u>OR</u>	2" x 2 condu with v auto p capab - secu clan - No pacl requ	" blac ctive vacuur ick ar ility: ure lid np) stacki ks. Si ured.	ck gel p m relo nd pla l (hin ing of	ack ease fo ace ge or f waffl clip	or e	
Microcircuit V elements b (integrated circuit dice)	Without air oridges	-] 2" coi wi - 0 4 1 1 - 1 1 - 5	No sta waffle clip re x 2" t nducti th: carrien deep e the die below of the protec pad secure clamp No sta	cking c packs. quired. plack ive waff well n enough e surfac the top waffle tive sho blid (hin) cking c	of Singl fle tray nust be so that e is o plane tray eet or nge or	le y t			OR	2" x 2 condu with v auto p capab - secu clar - No pacl requ	" blac ctive vacuun ick an ility: ure lid np) stacki ks. Si uired.	ck gel p m rela nd pla l (hin) ing of	ack ease fo ace ge or f waffl clip	or e	
v b	With air oridges		waffle Single	packs.	quired		<u>NLY</u>			2" x 2 condu with v auto p capab - secu clarr - No pacl requ	" blac ctive vacuun ick an ility: nre lid np) stacki ks. Si nired.	ck gel p m relo nd pla l (hin ing of ingle	ack ease fo ace ge or f waffl clip	or e	
For elements which will not fit into a 2" x 2" waffle tray or gel packElements shall be package1.Physically restrained physical damage or 2.2.Sealed in an electrose							d in a man from vibrat ectrical de tic bag.	ner that: tion and me gradation o	echanie f the e	cally isolement	olated s.	l fron	n shocl	k tha	at could cause
PROCUREMENT SPECIFICATION MICROCIRCUIT / SEMICONDUC							OR DR	1019- 1	618		V.	4	OF	7	DEPARIMENI

	DRAW 1019	ing no. -1618	REV. SHEET SCALE SIZE V 5 OF 7 NTS A										
5.0	PROC	EDURE:											
	5.1	<u>Conditio</u>	n A - Supplier requirements for semiconductor elements (transistor and diode dice).										
		5.1.1	The supplier shall perform 100% electrical testing at 25°C to ensure compliance to the manufacturer's electrical data book and/or element drawing. Devices shall be capable of operating over full temperature range to minimum and maximum electrical data book specifications/element drawing.										
		5.1.2	The supplier shall have an accepted internal document for visual inspection to MIL-STD-750, Method 2069, 2070, 2072, 2073 as applicable.										
		5.1.3	he supplier shall perform 100% visual inspection to an in-house control document in an environmentally ontrolled area and ensure compliance to all visual and mechanical specifications.										
		5.1.4	Element evaluation shall be performed by the supplier for each production lot in accordance with MIL-PRF-38534 for Class H elements.										
		5.1.5	Delivery Conditions:										
			a. <u>Packaging</u> - Packaging shall be IAW section 4.2 Packaging Requirements.										
			b. <u>Marking</u> - The dice type, manufacturer's name, quantity and wafer lot number shall appear on each waffle pack. All samples and test data shall be identified by its device type, manufacturer's name and wafer lot number. Markings shall be sufficient for inspection lot traceability.										
			 c. <u>Required Documentation</u> - Supplier performance data to be submitted with the inspection lot: 1. Attributes Data 2. Test Data 										
			d. <u>Certificate of Compliance</u> as defined in Document #81000.										
	5.2	<u>Conditio</u>	n A - Supplier requirements for microcircuit elements (integrated circuits).										
		5.2.1	The supplier shall perform 100% electrical testing at 25°C to ensure compliance to the manufacturer's electrical data book and/or element drawing. Devices shall be capable of operating over full temperature range to minimum and maximum electrical data book specifications/element drawing.										
		5.2.2	The supplier shall have an accepted internal document for visual inspection to MIL-STD-883 Method 2010 Condition B.										
		5.2.3	The supplier shall perform 100% visual inspection to an in-house approved control document in an environmentally controlled area and ensure compliance to all mechanical specifications.										
		5.2.4	Element evaluation shall be performed by the supplier on each wafer lot in accordance with MIL-PRF-38534 for Class H elements.										
		5.2.5	Delivery Conditions:										
			a. <u>Packaging</u> - Packaging shall be IAW section 4.2 Packaging Requirements.										
			b. <u>Marking</u> - The dice type, manufacturer's name, quantity and wafer lot number shall appear on each waffle pack. All samples and test data shall be identified by its device type, manufacturer's name and wafer lot number. Markings shall be sufficient for inspection lot traceability.										
			 c. <u>Required Documentation</u> - Supplier performance data to be submitted with the inspection lot: 1. Element Evaluation Data 2. Test Data 										
			d. <u>Certificate of Compliance</u> as defined in Document #81000.										
	5.3	<u>Conditio</u>	<u>n</u> B - Supplier requirements of all <u>semiconductor elements</u> (transistors and diode dice) and <u>microcircuit</u> (integrated circuits).										
		5.3.1	The supplier shall have an accepted internal document for Visual Inspection to MIL-STD-883 Method 2010 Condition B or MIL-STD-750 Method 2069, 2070, 2072, 2073 as applicable. The supplier shall perform visual inspection 100% in an environmentally controlled area and ensure compliance to all mechanical specifications.										
			PROCUREMENT SPECIFICATION FOR MICROCIRCUIT / SEMICONDUCTOR DRAWING NO. REV. SHEET DEPARTMENT 019-1618 V 5 OF 7										

DRAWING NO.	REV.	SHEET	SCALE SIZE
1019-1618	V	6 OF 7	NTS A

- **5.3.2** Each die shall be 100% electrically tested at 25°C to ensure compliance to the manufacturer's electrical database and/or element drawing. Devices shall be capable of operating over full temperature range to minimum and maximum electrical data book specifications.
- **5.3.3** Delivery conditions shall be in accordance with 5.1.5.
- 5.4 <u>Condition C</u> Elements procured for element drawing.
 - **5.4.1** The supplier shall perform 100% electrical testing at 25°C to manufacturers databook.

All electrical rejects shall be marked with solvent resistant ink.

Testing or grading for special electrical characteristics will be handled on an individual basis.

5.4.2 Devices shall be capable of meeting the visual requirements of MIL-STD-750 test method for semiconductor devices Method 2069, 2070, 2072, 2073 and MIL-STD-883 Method 2010 Condition B.

The contractor shall have a sample inspection performed on each wafer lot to assure conformance.

- 5.4.3 <u>Preservation</u>: Packaging shall be IAW section 4.2 Packaging Requirements
- 5.4.4 <u>Certificate of Compliance</u> as defined in Document #81000.
- 5.5 <u>Condition D and E</u> Supplier requirements for <u>semiconductor elements</u> (transistor and diode dice) and for <u>radiation</u> (as applicable) tested elements.
 - **5.5.1** The supplier shall perform 100% electrical testing at 25°C to ensure compliance to the manufacturer's electrical characteristics and/or element drawing. Devices shall be capable of operating over full temperature range to minimum and maximum electrical data book specifications/element drawing.
 - **5.5.2** The supplier shall have an accepted internal document for visual inspection to MIL-STD-883, Method 2069, 2070, 2072, 2073 as applicable.
 - **5.5.3** The supplier shall perform 100% visual inspection to an in-house control document in an environmentally controlled areas (see 3.6) and ensure compliance to all mechanical specifications.
 - **5.5.4** For Condition D Element evaluation shall be performed by the supplier for each wafer lot in accordance with MIL-PRF-38534 for Class K elements. <u>Test samples shall be delivered with each lot</u>.

For Condition E, Element evaluation shall be performed IAW the element drawing.

5.5.5 When specified on the purchase order, 12 die from the same lot shall be packaged and tested with recorded data. The packaged die shall be shipped prior to completion of Class K element evaluation. The 12 packaged die are above and beyond the Class K element evaluation and will be used for radiation testing.

5.5.6 <u>Delivery Conditions:</u>

- a. <u>Packaging</u> Packaging shall be IAW section 4.2 Packaging Requirements.
- b. <u>Marking</u> The die type, manufacturer's name, quantity and inspection lot number shall appear on each waffle pack. Markings shall be sufficient for inspection lot traceability.
- c. <u>Required Documentation</u> Supplier performance data to be submitted with the inspection lot:
 - 1. Element evaluation data.
 - 2. Test data (Space Data Package, as applicable)
- d. <u>Certificate of Compliance</u> as defined in Document #81000.
- 5.6 <u>Condition D and E</u> Supplier requirements for <u>microcircuit elements</u> (Integrated Circuits) and for <u>radiation</u> (as applicable) tested elements.
 - **5.6.1** The supplier shall perform 100% electrical testing at 25°C to ensure compliance to the manufacturer's electrical characteristics and/or element drawing. Elements shall be capable of operating over full temperature range to minimum and maximum electrical data book specifications/element drawing.

PROCUREMENT SPECIFICATION FOR	DRAWING NO.	REV.	SHEET	DEPARTMENT
MICROCIRCUIT / SEMICONDUCTOR	1019-1618	V	6 OF 7	

	DRAW	/ING NO.		REV.	SI 7 (SCALE					
	1013	562	The	suppl	ier sh	all have		cented	internal document for visual inspection to MIL-STD-883 Method 2010			
		5.0.2	Con	dition	A.	an nave		cepieu	internal document for visual hispection to with-51D-885 method 2010			
		5.6.3	The envi	suppl ronme	ier sh entally	all perfo y contro	orm 10 olled ar	00% vi rea (Se	sual inspection to an in-house approved control document in an se 3.6) and ensure compliance to all mechanical specifications.			
		5.6.4	For MIL	Condi PRF	tion I -3853	D Eleme 34 for C	ent eva lass K	luation	n shall be performed by the supplier for each wafer lot in accordance with nts. <u>Test samples shall be delivered with each lot</u> .			
			For	Condi	tion E	E Eleme	nt eva	luatior	n shall be performed IAW the element drawing.			
		5.6.5	Whe data die a	en spe . The are abo	cified packa	l on the aged die nd beyo	purcha e shall nd the	ise ord be shi Class	er, 12 die from the same lot shall be packaged and tested with recorded pped prior to completion of Class K element evaluation. The 12 packaged K element evaluation and will be used for radiation testing.			
		5.6.6	Deli	livery Conditions:								
			a.	Packa	aging	- Pack	aging	shall b	e IAW section 4.2 Packaging Requirements.			
			b.	<u>Mark</u> waffle	t <mark>ing</mark> - e pack	The dik. Mark	ie type tings sl	, manı hall be	facturer's name, quantity and inspection lot number shall appear on each sufficient for inspection lot traceability.			
			c.	Requ 1. E	ired l Eleme	Docum int evalu	entation of	<u>on</u> - Su data.	upplier performance data to be submitted with the inspection lot:			
			1	2. T	est da	ata (Spa	ice Dat	ta Pacl	cage, as applicable)			
			a.	Certi	icate	<u>oi Com</u>	plianc	<u>e</u> as de	enned in Document #81000.			
6.0	<u>ACCE</u>	EPT/REJI	ECT C	RITE	RIA:	<u>!</u>						
	6.1	Accept a	ull lots v	which	pass	the app	licable	parag	raphs of this procedure and the element drawing.			
	6.2	Reject a	Reject any device(s) and separate it from the lot which fails an electrical parameter or visual/mechanical criteria.									
	6.3	Reject a	ny wafe	er lot v	which	does n	ot pass	eleme	ent evaluation or radiation testing.			
7.0	<u>QUAI</u>	LITY ASS	SURAN	NCE P	ROV	ISION	<u>'S:</u>					
	7.1	Anaren 1 requiren	reserves nents of	s the r f this c	ight to locum	o perfor nent sha	rm test ll be c	ing in ause fo	accordance with paragraph 2.0 and any failure of the material to meet or rejection.			
	7.2	Anaren 1 this spec	eserve	s the r on, the	ight to purcl	o reviev hase orc	v any s ler and	supplie l the el	ers program, process and data to assure conformance to the requirements of ement drawing.			
8.0	<u>REFE</u>	RENCE	DOCU	MEN	TS:							
	8.1	MIL-ST	D-883									
	8.2	Element	drawin	ıg.								
	8.3	Anaren j	ourchas	se orde	er.							
	8.4	MIL-ST	D-750									
	8.5	MIL-PR	F-3853	4								
	8.6	MIL-PR	F-1950	00								
	8.7	MIL-PRF-38535										
	8.8	ISO14644-1, -2 or MIL-STD-209										
	8.9	Anaren	supplier	r requi	ireme	ents for (Quality	y, Desi	gn & Manufacturing, Document #81000.			
			PRO MIC	CUREI		SPECIF		ON FOF	DRAWING NO. REV. SHEET DEPARTMENT 1019-1618 V 7 OF 7			