CoreEZ®

CoreEZ® semiconductor package uses the HyperBGA® manufacturing platform to offer a thin core build up flip chip package with very dense core vias using a cost sensitive material set. The core via density provides 199 micron via to via core pitch, resulting in an essentially coreless structure.

High core via density is achieved using smaller pads and the same 50 micron laser drilled holes used in producing HyperBGA® to unblock wiring channels through the core. This enables CoreEZ® to provide up to twice the number of signal layers as a standard build up package that uses mechanically drilled core vias with large capture pads.

The end result is an extremely cost effective solution that allows full strip line signal layers on both sides of the core. Component cost is further reduced by enabling die shrink through die pad pitch reduction down to 150 microns.

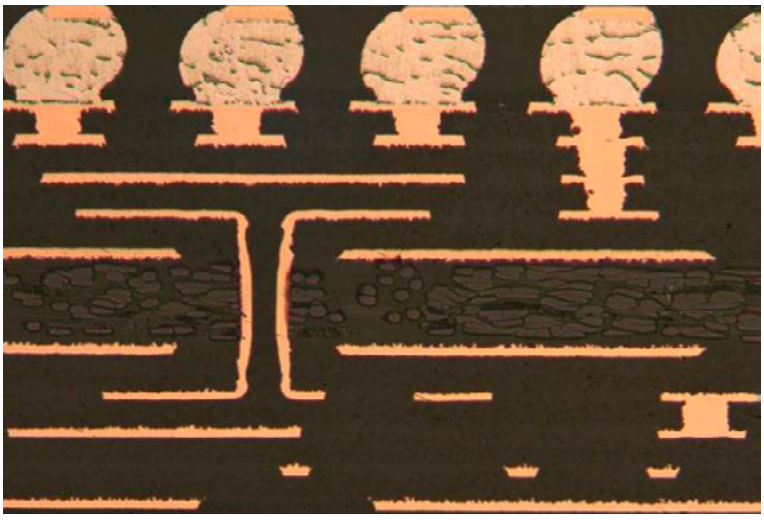
In addition, the thinness of the core provides improved power distribution and the ability to dissipate chip thermal power into the PCB.

CoreEZ® is an excellent choice for applications requiring low cost build up materials along with high reliability, performance and wireability. It is also well suited to aerospace applications requiring radiation tolerance.

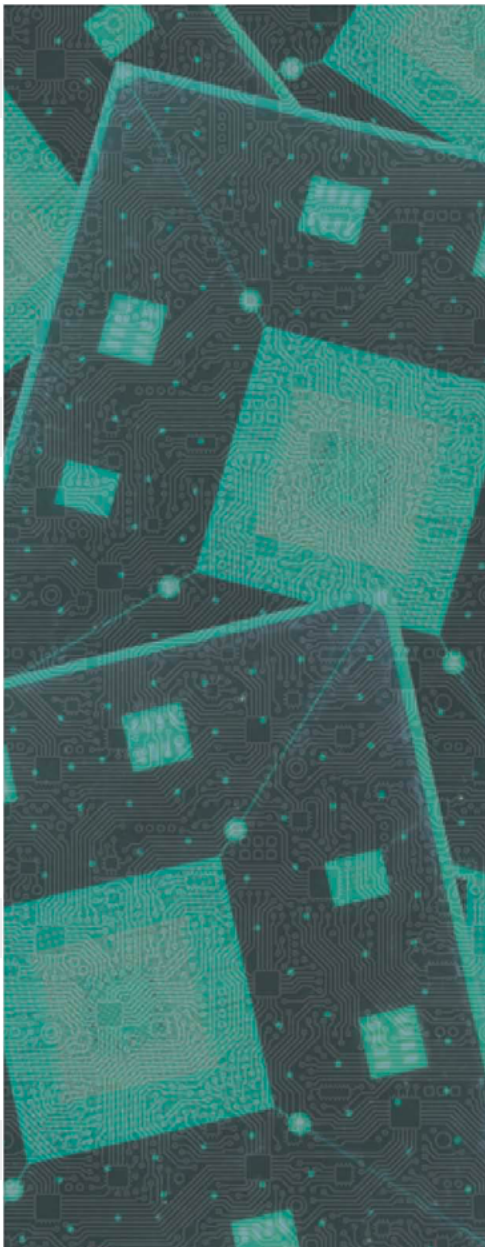
DESCRIPTION

Up to 12 layer Particle Filled Epoxy Substrate

- Great solution for PCBA to SiP redesigns
- Very dense core vias (<200 micron pitch)
- 50 micron UV laser drilled vias
- 25 micron trace/33 micron space
- High reliability
- Rad Hard



CoreEZ® SPECIFICATIONS



LAMINATE

Line width	25 µm minimum
Line space	25 µm minimum
Pad diameter	100 µm minimum
Via diameter	50 µm minimum (UV laser drilled)
Minimum die pad pitch	150 µm
Build-up dielectric thickness	35 µm, 50 µm

MATERIALS

All Planes	Copper
Dielectrics	P-Aramid in core and silica-filled high Tg epoxy Resin-Coated Copper
Outer Dielectric	Low-loss thermoset dielectric
Ground Plane	Copper-invar-copper
Flip chip Pad Surface Finish	Eutectic on ENIG, ENIG, lead free compatible on ENIG
Wirebond Compatible	ENEPIG
BGA metallurgy	ENIG on copper, OSP on copper
ENEPIG Available	for wirebond
BGA Metallurgy ENIG	ENIG on Copper, OSP on Copper, (ENIG) lead free compatible on ENIG

ELECTRICAL

Build-up layer dielectric constant	3.7 up to 2.5 GHz
Build-up layer loss	0.013 to 1 MHz
Core material dielectric constant	3.7 up to 2.5 GHz
Core material dielectric loss	0.018 at 1 MHz

PHYSICAL

Single chip body sizes	JEDEC up to 55.0 mm
System-in-package body size	Custom
Number of I/Os	Up to 2916 at 1.0 mm smaller pitch possible

REALIBILITY STRESS TESTING

Board level thermal cycles	Over 4,000 cycles of 0˚ to 100˚C
High-temperature storage	150˚C for 1,000 hours
Component level thermal cycles	1,000 cycles of -55˚ to 125˚C

Results may vary with different die, assembly processing or design attributes.

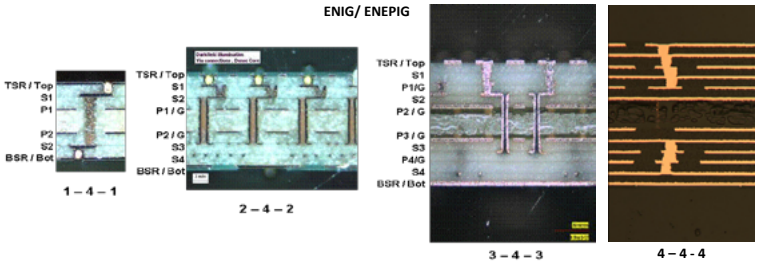
Inspiring Innovation
www.ttm.com
follow us on

TTM Technologies

CoreEZ®

CoreEZ® IS AVAILABLE AS A 1-4-1, 2-4-2 , 3-4-3 OR 4-4-4 CROSS SECTIONS

- 1-4-1 = 2 full stripline signal planes, 4 pwr/gnd
- 2-4-2 = 4 dual stripline signal planes, 4 pwr/gnd
- 3-4-3 = 4 full stripline signal planes, 6 power/gnd
- 4-4-4 = 4 full stripline signal planes, 8 pwr/gnd



Attribute	HDI: Hyper® (PTFE)	HDI: CoreEZ® (Particle Filled Epoxy)
PCB Attach	BGA, Custom Pin Array	BGA, Custom Pin Array
Die attach	Wirebondable, Flip Chip up to 20mm, SMT	Wirebondable, Flip Chip up to 17mm, SMT
Radiation Level	Rad Tolerant	Strategic Rad Hard
Embedded Passives	Yes	Yes
FC Component level reliability (-55 to 125*C)	250 cycles	1000 cycles
FC Board level reliability (0 to 100*C)	10,000 cycles	5,000 cycles
Composite CTE	16-18ppm	18ppm, 16ppm for 2-4-2
Er	2.7	3.7
Loss Tan	.003	.016

SUBSTRATE PRODUCT ATTRIBUTES

Attribute	HDI: CoreEZ® (Particle Filled Epoxy)
C4 Pitch (Minimum)	180 microns nominal, 150 µm possible for specific applications
Line width (Minimum)	25 microns *
Line space (Minimum)	30 microns *
Core Via type	laser
Core Via Diameter	50 microns
Build Up Via	laser
Build Up Via diameter	50 microns
Stacked vias	Build up only
Capture pad diameter (Typical)	100 microns
Surface finish	ENIG/ ENEPIG
Solder mask	Yes
Thickness	.5mm
Layers	12

CoreEZ®

CoreEZ® RELIABILITY TESTING

Stress Test	Duration Required to Pass	2-4-2 Substrates	2-4-2 Modules 14.7mm Die / 42.5 Pkg	3-4-3 Modules 17.3 Die / 42.5 Pkg	4-4-4 Substrates	4-4-4 Modules 17.3 Die / 50 Pkg
Board level (ATC) (0 to 100°C)	3600 Cycles	No fails @ 3600 cycles	No fails @ 5000 cycles	No fails @ 3500 cycles	No fails @ 5000 cycles	
Component level (DTC) (-55 to + 125°C)	1000 Cycles	No fails @ 2000 cycles		No fails @ 2000 cycles	No fails @ 2000 cycles	No fails @ 2000 cycles
Component level (DTC) (-40 to + 125°C)	1000 Cycles	No fails @ 2000 cycles		No fails @ 2000 cycles		
Component level (DTC) (-55 to + 110°C)	1000 Cycles			No fails @ 2000 cycles		
Wet Thermal Shock (-55 to + 125°C)	100 Cycles	No fails @ 2000 cycles			No fails @ 1000 cycles	No fails @ 750 cycles
High Temp Storage (150°C)	1000 hours				No fails @ 1000 hours	No fails @ 1000 hours
High Temp Storage (125°C)	1000 hours	No fails @ 2023 hours				
Unbiased HAST (110°C / 85% RH)	264 hours	No fails @ 264 hours			No fails @ 264 hours	No fails @ 288 hours
Temp/Humidity & Bias (85°C / 85%RH / 3.7V	1000 hours	No fails @ 1000 hours				
High Temp Operating Life 125C/3.5vdc/1000hrs	1000 hours				1000 hrs no fails	