MIL-PRF-38534 AND 38535 CERTIFIED FACILITY

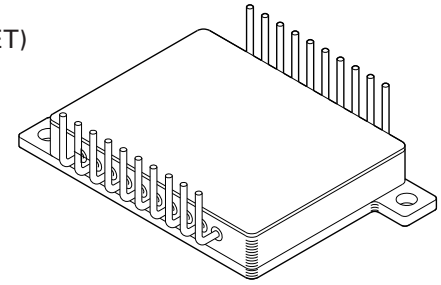
M.S.KENNEDY CORP.

10 AMP, 100 VOLT RAD HARD MOSFET POWER 3-PHASE MOTOR DRIVE HYBRID

4304RH

FEATURES:

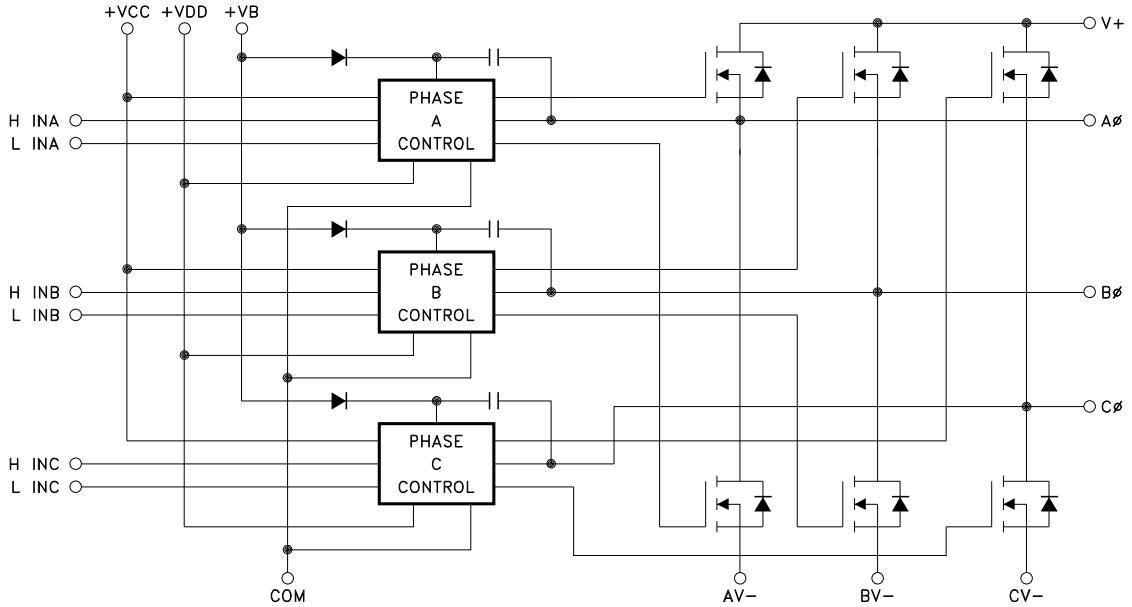
- 100V, 10 Amp Capability
- Ultra Low Thermal Resistance - Junction to Case - 2.5°C/W (Each MOSFET)
- Self-Contained, Lowside/Highside Drive Circuitry
- Bootstrap High-Side Supplies
- Under-Voltage Lockout
- Capable of Switching Frequencies to 25KHz
- Isolated Case Allows Direct Heat Sinking
- Bolt-down Design Allows Superior Heat Dissipation
- Total Dose Hardened to 300 Krads(Si) (Method 1019.7 Condition A)



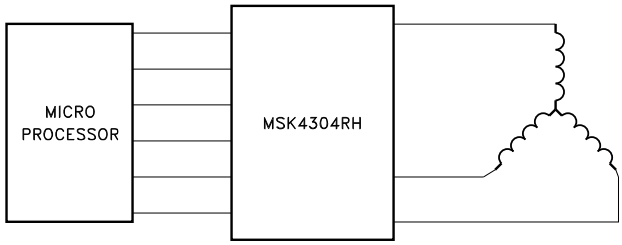
DESCRIPTION:

The MSK4304RH is a radiation hardened 10 Amp, 3 Phase Bridge Power Motor Drive Hybrid with a 100 volt maximum rating on the output switches. The internal components have been selected to provide total dose tolerance for military and space applications. The output switches are MOSFETs. This new power motor drive hybrid is 5.0 volt input logic compatible. Under-voltage lockout prevents the bridge from starting before the supply voltage rises high enough for complete turn-on of the output switches. The internal high-side bootstrap power supply derived from the +VB supply completely eliminates the need for 3 floating independent power supplies.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS



3 PHASE SIX STEP DC BRUSHLESS MOTOR DRIVE
OR 3 PHASE SINUSOIDAL INDUCTION MOTOR DRIVE

PIN-OUT INFORMATION

1	H INA	20	V+
2	L INA	19	N/C
3	+VCC	18	AV-
4	H INB	17	AØ
5	L INB	16	N/C
6	COM	15	BV-
7	+VDD	14	BØ
8	+VB	13	N/C
9	H INC	12	CV-
10	L INC	11	CØ

CASE = ISOLATED

ABSOLUTE MAXIMUM RATINGS ⑦

V+	High Voltage Supply ⑨	100V	I_{PK}	Peak Output Current	14A
+VDD	Logic Supply	18V	TsT	Storage Temperature Range ⑩	-65° to +150°C
$V_{H/LIN}$	Logic Input Voltage	V_{DD}	TLD	Lead Temperature Range	
$I_{H/LIN}$	Logic Input Current	10mA	TC	(10 Seconds)	300°C
+VCC	Lowside Supply	18V		Case Operating Temperature	
+VB	Highside Supply	18V		MSK4304RH	-40°C to +85°C
I_{OUT}	Continuous Output Current	10A		MSK4304KE/HE RH	-40°C to +125°C
θ_{JC}	Thermal Resistance @ 125°C (Output Switches, Junction to Case)	2.5°C/W	TJ	Junction Temperature	+150°C

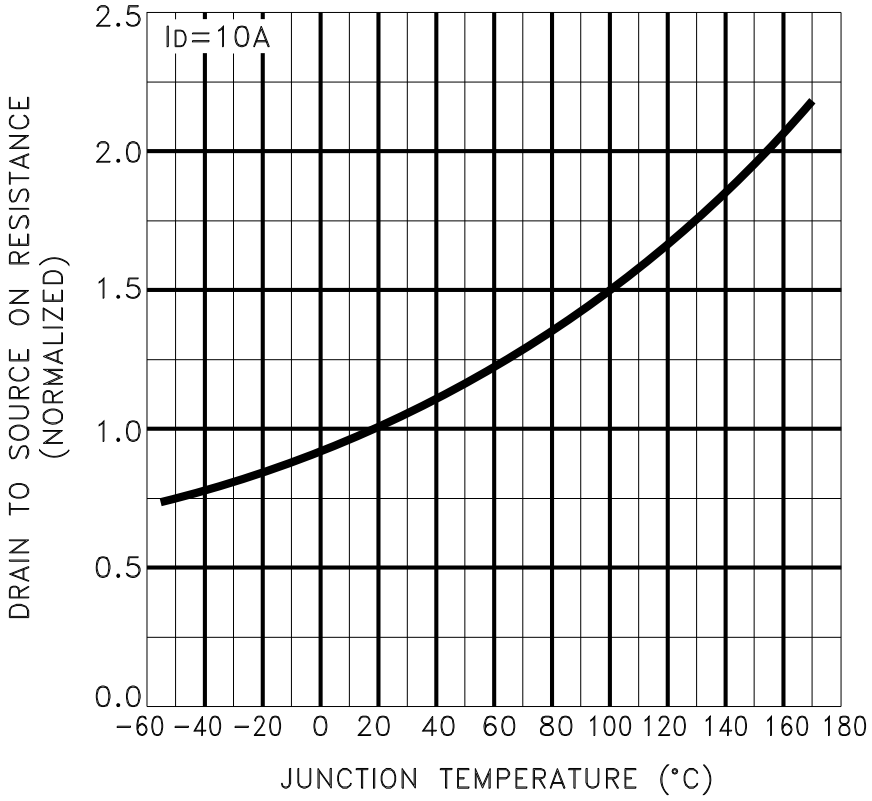
ELECTRICAL SPECIFICATIONS

Parameters	Test Conditions ⑧		GROUP A SUBGROUP ⑤	MSK4304KE/HE RH ③ Min.	Typ.	Max.	MSK4304RH ② Min.	Typ.	Max.	UNITS
OUTPUT CHARACTERISTICS										
Drain-Source ON Resistance ① (each MOSFET) (for thermal calculations only)	I_{DS} = 10A		1	-	-	0.08	-	-	0.08	Ω
			2	-	-	0.16	-	-	-	Ω
			3	-	-	0.08	-	-	-	Ω
Drain-Source Voltage (VDS(on)) (each MOSFET)	I_{DS} = 10A		1	-	0.8	1.5	-	0.8	1.6	volts
			① 2	-	1.4	2.4	-	-	-	volts
			① 3	-	0.6	1.2	-	-	-	volts
Leakage Current (Each MOSFET)	V+ = 80V		1	-	1	25	-	1	25	μA
	V+ = 80V		2	-	10	250	-	-	-	μA
	V+ = 80V		3	-	1	25	-	-	-	μA
Reverse Recovery Time ①	I_D = 10A, di/dt = 100A/μS		-	-	-	370	-	-	370	nS
BODY DIODE CHARACTERISTICS										
V_{SD} Diode Forward Voltage ①	I_S = 18A, V_{GS} = 0V		1	-	-	1.2	-	-	1.2	V
T_{RR} Reverse Recovery Time ①	I_F = 18A		1	-	-	250	-	-	250	ns
Q_{RR} Reverse Recovery Charge ①	di/dt < 100A/us, VDD < 25V		1	-	-	850	-	-	850	nC
BIAS SUPPLY CHARACTERISTICS										
+VCC Bias Current	+VCC = 15V		1,3	-	0.02	2	-	0.02	2	mA
			2	-	-	6	-	-	6	mA
+VB Bias Current	+VB = 15V		1,3	-	0.02	2	-	0.02	2	mA
			2	-	-	6	-	-	6	mA
+VDD Bias Current	+VDD = 15V		1,2,3	-	4.5	9	-	4.5	9	mA
INPUT SIGNAL CHARACTERISTICS										
Positive Trigger Threshold Voltage	+VCC = 15V		1,2,3	-	2.3	3.0	-	2.3	3.0	volts
Negative Trigger Threshold Voltage	+VCC = 15V		1,2,3	0.8	1.8	-	0.8	1.8	-	volts
Under-voltage Lockout ⑥	+VDD		1,2,3	8.0	10	12.0	8.0	10	12.0	volts
Logic Input Current	All Inputs	V_{IN} = +5V	1,2,3	-	25	75	-	25	75	μA
		V_{IN} = 0V	1,2,3	-10	-1.2	-	-10	-1.2	-	μA
Switching Loss Inductive Load ①		E(ON)	4	-	TBD	-	-	TBD	-	μJ
		E(OFF)	4	-	TBD	-	-	TBD	-	μJ

NOTES:

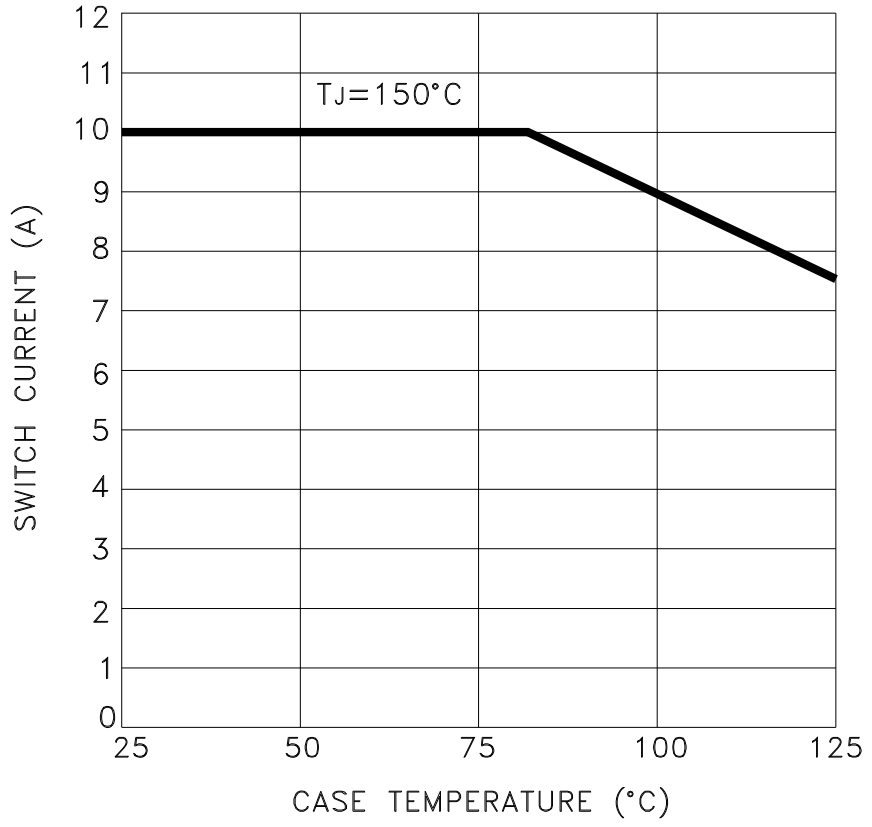
① Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
② Industrial grade devices shall be tested to subgroups 1 unless otherwise specified.
③ Space and Military grade devices ("KE & HE" suffix) shall be 100% tested to subgroups 1, 2 and 3.
④ Subgroups 5 and 6 testing available upon request.
⑤ Subgroup 1, 4 TA = TC = +25°C
2, 5 TA = TC = +125°C
3, 6 TA = TC = -40°C for 'KE' and 'HE' SUFFIXES
⑥ See UVLO paragraph in the application notes section.
⑦ Continuous operation at or above absolute maximum ratings may adversely effect the device performance and/or life cycle.
⑧ Pre and post irradiation limits at 25°C, up to 300Krad TID, are identical unless otherwise specified.
⑨ When applying power to the device, apply the low voltage followed by the high voltage or alternatively, apply both at the same time. Do not apply high voltage without low voltage present.
⑩ Internal solder reflow temperature is 180°C, do not exceed.

TYPICAL PERFORMANCE CURVE



SAFE OPERATING AREA

SWITCH CURRENT vs CASE TEMPERATURE



APPLICATION NOTES

MSK 4304RH PIN DESCRIPTIONS

+VCC - Is the low voltage supply for the lowside drivers. A 0.1 μF ceramic capacitor in parallel with a 10μF tantalum capacitor is the recommended bypassing from the +VCC pin to the COM pin.

+VDD - Is the low voltage supply for the input logic to the hybrid. A 0.1 μF ceramic capacitor in parallel with a 4.7μF tantalum capacitor is the recommended bypassing to the COM pin.

+VB - Is the connection used to provide power to the floating high-side bootstrap supplies in the gate drive circuitry.

V+ - Is the high voltage positive rail connection to the tops of the three half bridges. Proper power supply bypassing must be connected from this pin to the COM pin for good filtering. This bypassing must be done as close to the hybrid as possible. +VCC, +VDD and +VB should be present and stable whenever V+ is present.

H INA, H INB, H INC - Are active high logic inputs for signalling the corresponding phase high-side switch to turn on. The logic inputs are compatible with standard LSTTL/CMOS outputs. These inputs are clamped to VDD and COM, they must be limited to less than 10mA if they are allowed to exceed those limits.

L INA, L INB, L INC - Are active high inputs for signalling the corresponding phase low-side switch to turn on. The logic inputs are compatible with standard LSTTL/CMOS outputs. These inputs are clamped to VDD and COM, they must be limited to less than 10mA if they are allowed to exceed those limits.

AØ, BØ, CØ - Are the pins connecting the 3 phase bridge switch outputs.

AV-, BV-, CV- - Are the connections from the bottoms of the three half bridges. These pins get connected to the COM pin. If current sensing is desired they may be connected to the COM pin through a low value sense resistor.

COM - Is the connection that all hybrid power supply connections are returned to and bypassed to.

UVLO - The under voltage lockout function of the MSK4304RH prevents the device from starting before sufficient bias voltage is available. The UVLO feature monitors the VDD supply and holds the outputs low until the voltage level rises above the threshold during start up. After start up the UVLO circuit will hold the low side switches off if VDD falls below the threshold but the high side switches will not be controlled by UVLO after start up.

MAXIMUM DUTY CYCLE AND HIGH SIDE BIAS - The MSK4304RH uses three independent bootstrap circuits to power each of the high side switches. When the switches are turned on the high side drivers are powered by the charge in the bootstrap capacitors. The voltage on the bootstrap capacitors has an initial 1.2V drop and decays at a rate of approximately 0.5V every 100μS. The voltage can be approximated by the equation:

$$V_{BS} = +VB - 1.2V - 5 \times T_{ON}$$

T_{ON} is the switch on time in mS
V_{BS} is the bootstrap capacitor voltage

V_{BS} should be greater than or equal to 10 volts for maximum gate drive. If V_{BS} falls too low loss of high side control my result.

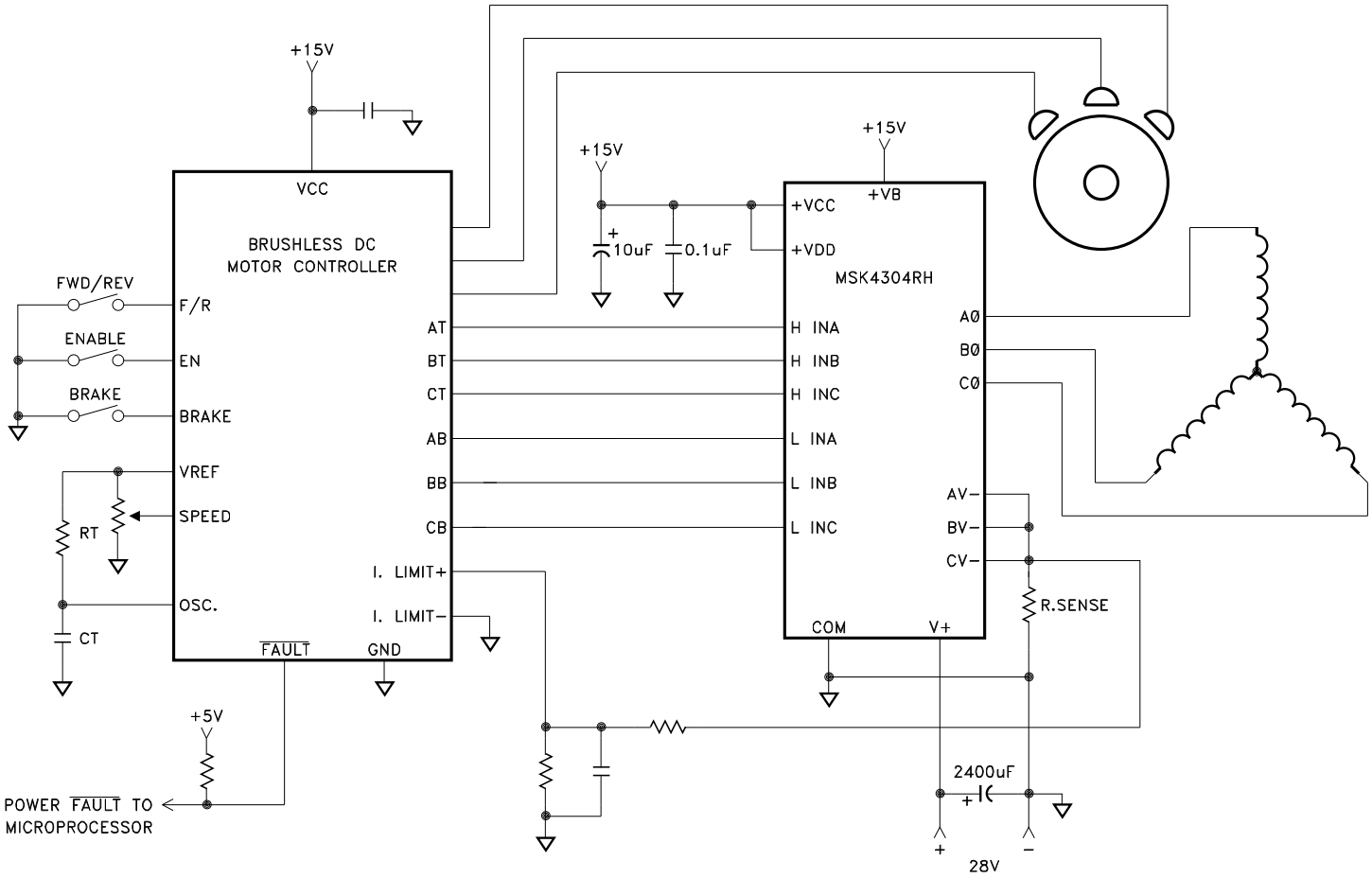
The lowside switches must be activate every cycle or held active during static operation to provide a return path for charging the highside bootstrap capacitor and prevent loss of highside control.

TOTAL DOSE RADIATION TEST PERFORMANCE

Radiation performance curves for TID testing have been generated for all radiation testing performed by MS Kennedy. These curves show performance trends throughout the TID test process and can be located in the MSK4304RH radiation test report. The complete radiation test report is available in the RAD HARD PRODUCTS section on the MSK website.

http://www.mskennedy.com/store.asp?pid=9951&catid=19680

TYPICAL SYSTEM OPERATION



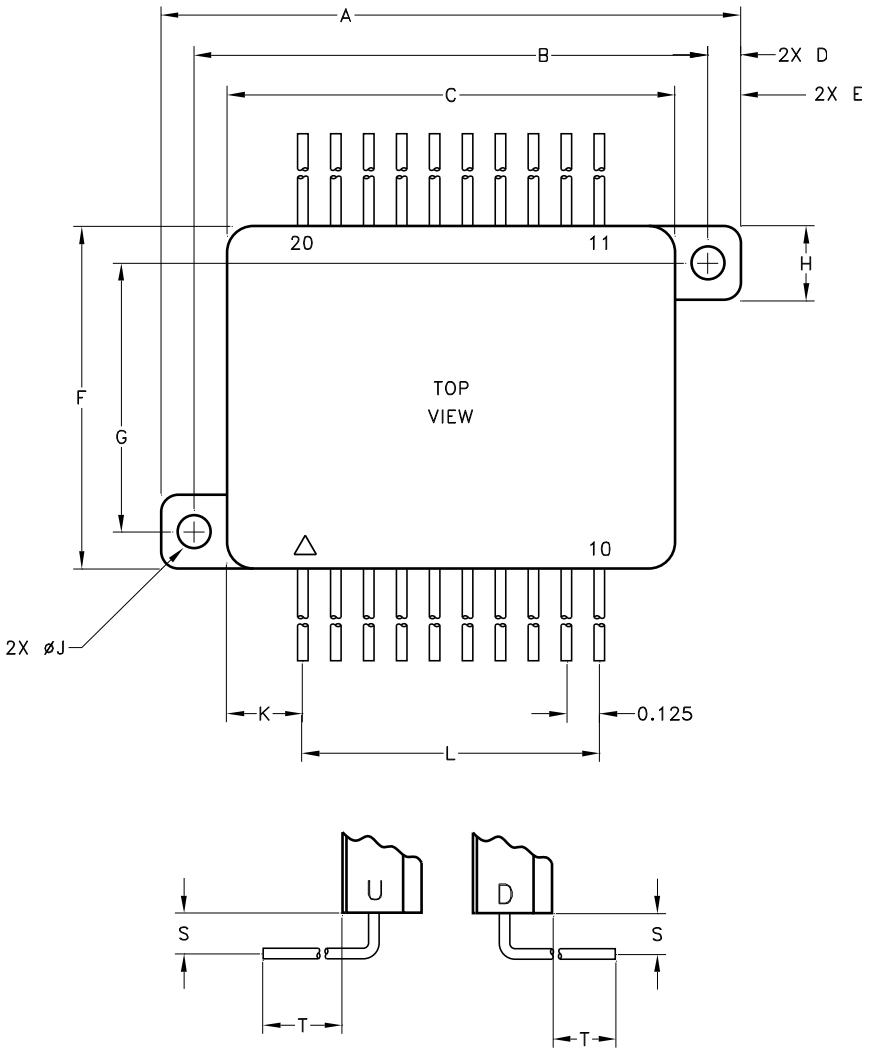
The MSK4304RH is designed to be used with a +28 volt high voltage bus, +15 volt low power bus and +5 volt logic signals. Proper derating should be applied when designing the MSK4304RH into a system. High frequency layout techniques with ground planes on a printed circuit board is the only method that should be used for circuit construction. This will prevent pulse jitter caused by excessive noise pickup on the current sense signal or the error amp signal.

Ground planes for the lower power circuitry and the high power circuitry should be kept separate. The connection between the bottom of the current sense resistor, COM pin and the high power ground, AV-, BV- and CV- pins are connected at this point. This is a critical path and high currents should not be flowing between the current sense and COM. Inductance in this path should be kept to a minimum. An RC filter will filter out the current spikes and keep the detected noise for those circuits down to a minimum.

In the system shown a PWM pulse by pulse current limit scheme controlled by the motor controller is implemented.

When controlling the motor speed by the PWM method, it is required that the low side switches be PWM pulsed to ensure sufficient bootstrap capacitor charge to power the high side switch drives. The higher the PWM speed the higher the current load on the drive supply.

MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	2.190	2.210
B	1.940	1.960
C	1.690	1.710
D	0.115	0.135
E	0.240	0.260
F	1.290	1.310
G	1.040	1.060
H	0.270	0.290
J	0.120	0.130
K	0.278	0.298
L	1.115	1.135
M	0.500	—
N	—	0.300
O	0.050	0.070
P	0.035	0.045
R	0.150	0.170
S	0.120	0.130
T	0.175	—

ESD TRIANGLE INDICATES PIN 1
WEIGHT = 42 GRAMS TYPICAL

CONTAINS INTERNAL BeO (BERYLLIUM OXIDE)
ALL DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

MSK4304 __ RH U

LEAD CONFIGURATIONS
S = STRAIGHT; U = BENT UP; D = BENT DOWN

SCREENING
BLANK = INDUSTRIAL; HE = MIL-PRF-38534 CLASS H (REDUCED TEMP);
KE = MIL-PRF-38534 CLASS K (REDUCED TEMP);

GENERAL PART NUMBER

REVISION HISTORY

REV	STATUS	DATE	DESCRIPTION
J	Released	08/14	Remove GBD note from trigger threshold voltage.

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