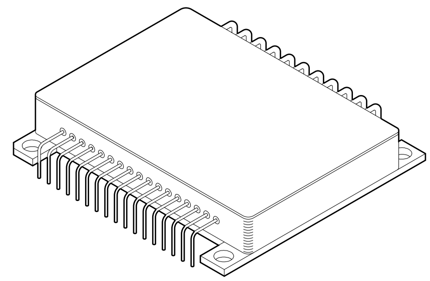
MSK

RAD HARD 10 AMP, 70V, H-BRIDGE MOSFET STEPPER MOTOR DRIVE

4231RH

FEATURES:

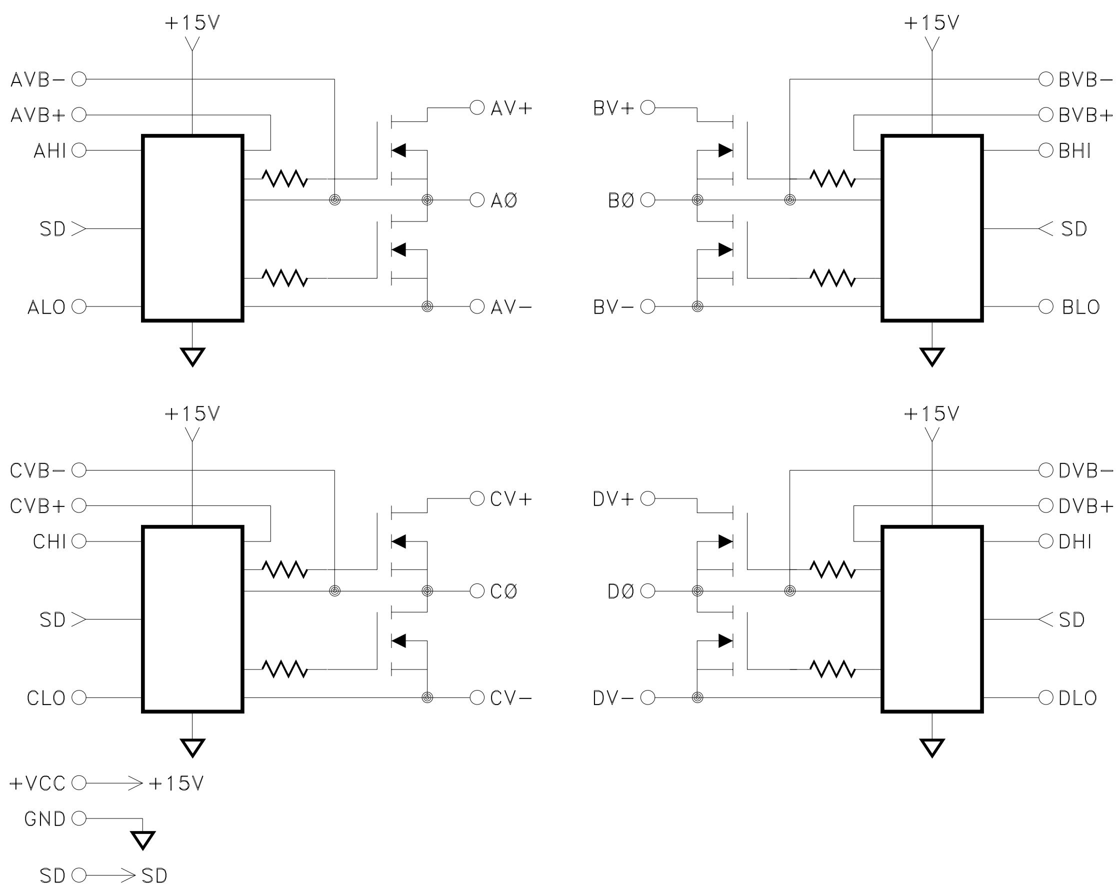
- Total Dose Hardened to 100 Krads(Si) (Method 1019.7 Condition A)
- 70V Maximum Operating Motor Supply Voltage
- 100V Absolute Maximum Output Stage Rating
- 10Amp Continuous Output Switch Capability
- Two Independent H Bridge MOSFET Output Stages Plus Gate Drivers
- External High Side Capacitor Connections for Extended High Side Operation
- Provisions for Bottom Side Current Sensing
- Logic Level Bridge Shutdown
- Isolated Package Design for High Voltage Isolation Plus Good Thermal Transfer
- Contact MSK for MIL-PRF-38534 Qualification and Radiation Test Status
- Non-Rad Hard EDU Version Available (MSK4230)



DESCRIPTION:

The MSK4231RH is a rad hard dual, independent MOSFET H Bridge with gate drivers for dual winding stepper motor drive capability. It is constructed in a convenient isolated hermetic package. The logic input and bridge output have a common return; the input is not electrically isolated from the output. Provisions for output stage isolation must be made externally. Each high side drive has the capability of connecting external capacitance for extended high side ON time before refresh is necessary. A common shutdown pin will disable both bridges upon activation. The bridge is capable of 10Amp continuous current output with sufficient heat sinking, and is capable of 70V maximum operating supply voltage. The bridge is constructed with 100V absolute maximum voltage rated MOSFET to allow for de-rating to 70V. Any PWM scheme can be used for any type of microstepping for both high torque and/or high speed motor operation. There is no simultaneous conductive lockout, so provisions must be made externally for dead time. The MSK4231RH has good thermal conductivity for output stage power dissipation due to the isolated package design that allows direct heat sinking of the device without insulators.

EQUIVALENT SCHEMATIC



8548-152 Rev. A 2/15

PIN-OUT INFORMATION

1 AVB+	9 BVB-	17 DHI	25 CV+
2 AHI	10 +VCC	18 DLO	26 NC
3 ALO	11 GND	19 DVB-	27 BV-
4 AVB-	12 CVB+	20 DV-	28 BØ
5 SD	13 CHI	21 DØ	29 BV+
6 BVB+	14 CLO	22 DV+	30 AV-
7 BHI	15 CVB-	23 CV-	31 AØ
8 BLO	16 DVB+	24 CØ	32 AV+

ABSOLUTE MAXIMUM RATINGS ⑥

A, B, C, DV+(V_{DD})	High Voltage Supply ⑦	100V
+VCC	Logic Supply	16V
I_{OUT}	Continuous Output Current	10A
I_{PK}	Peak Output Current	16A
A, B, C, DHI; A, B, C, DLO, SD	Logic Input Voltage	15V or +VCC whichever is lower
$R_{\theta JC}$	Thermal Resistance (output switches, junction to case @ 125°C)	3.9°C/W
T_{ST}	Storage Temperature Range ⑨	-65°C to +150°C
T_{LD}	Lead Temperature Range (10 Seconds)	300°C
T_C	Case Operating Temperature	
	MSK4231RH	-40°C to +85°C
	MSK4231K/HRH	-55°C to +125°C
T_J	Junction Temperature	+150°C

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions	Group A Subgroup	MSK4231K/HRH Min.	MSK4231K/HRH Typ.	MSK4231K/HRH Max.	MSK4231RH Min.	MSK4231RH Typ.	MSK4231RH Max.	Units
V_{DS}(on)	ID=10A	1	–	0.56	1.06	–	0.56	1.16	V
		2	–	1.01	1.86	–	–	–	V
		3	–	0.9	1.06	–	–	–	V
R_{DS}(on) (Each FET, for thermal calculations only) ①		–	–	–	50	–	–	50	mOhm
Leakage Current	V_{DS}=80V	1	–	TBD	TBD	–	TBD	TBD	mA
		2	–	TBD	TBD	–	TBD	TBD	
		3	–	TBD	TBD	–	TBD	TBD	
Diode V_{SD} ①	I_{SD}=10A	–	–	–	1.8	–	–	1.8	V
Diode Trr ①	I_{SD}=10A	–	–	TBD	–	–	TBD	–	nS
Delay Time-XLO/HI to XØ	V_{DD}=28V, 20kHz	4	–	TBD	–	–	TBD	–	uS
		5	–	TBD	–	–	–	–	uS
		6	–	TBD	–	–	–	–	uS
Shutdown Delay SD to XØ	V_{DD}=28V, 20kHz	4	–	TBD	–	–	–	–	uS
		5	–	TBD	–	–	–	–	
		6	–	TBD	–	–	–	–	
Quiescent Current	+VCC=+15V, V_{DD}=0V	1	–	TBD	–	–	–	–	mA
		2	–	TBD	–	–	–	–	
		3	–	TBD	–	–	–	–	
Operating Current ①	+VCC=+15V, V_{DD}=28V ID=10A PWM All XLO/HI=20kHz	–	–	TBD	–	–	–	–	mA
Logic Input ①									
V_{IH}	+VCC=15V	–	9.5	–	–	9.5	–	–	V
V_{IL}		–	–	–	5.7	–	–	5.7	V

NOTES:

① Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
② Industrial grade devices shall be tested to subgroup 1 and 4 unless otherwise specified.
③ Military grade devices ('H' and 'K' suffix) shall be 100% tested to subgroups 1,2,3 and 4.
④ Subgroups 5 and 6 testing available upon request.
⑤ Subgroups 1,4 TA=TC=25°C
2,5 TA=TC=125°C
3,6 TA=TC=-55°C
⑥ Continuous operation at or above absolute maximum ratings may adversely effect the device performance and/or life cycle.
⑦ When applying power to the device, apply the low voltage followed by the high voltage or alternatively, apply both at the same time. Do not apply the high voltage without the low voltage present.
⑧ Pre and post irradiation limits @ 25°C, up to 100Krad TID, are identical unless otherwise specified.
⑨ Internal solder reflow temperature is 180°C, do not exceed.

APPLICATION NOTES

AV+, BV+, CV+, DV+ - Are the main output stage positive power pins. Traces shall be designed for the required current. It is very important to place proper bypass capacitors as close to the V+ pins and either the V- or sense resistor return pins as close to the module as possible. Good quality bulk capacitors of at least 10uF per amp of required current, 1uF ceramic and a good high frequency polyester or mylar capacitor of at least 3.3uF shall be used. The poly or mylar capacitor will serve as a very low ESR capacitor for the high frequency transients present from switching the output stage, and help compensate for stray inductance in the power paths.

AV-, BV-, CV-, DV- - Are the main output stage positive power return pins. Traces shall be designed for the required current. DC link current sense resistor shall connect to this point, as close to the module as possible for the least stray inductance. At a minimum, use a non-inductive resistor, and preferably the four wire sense variety for the best sensing without the effect of voltage drops due to current. If a sense resistor is not used, connect this point to the power return with a minimum of trace inductance, and terminate the power bypass capacitors at this point as close to the module pins as possible. A wide output ground plane section is recommended to connect up all of the power return pins if current sense resistor are not used. If they are used, then minimum trace length to the resistor, and then an output ground plane section shall be used to collect all of the resistor negative return points. All output bypass capacitors shall connect to this ground plane as well.

AØ, BØ, CØ, DØ - Are the half bridge output pins. Traces shall be designed for the required current.

AHI, BHI, CHI, DHI - Are the logic pins for controlling the high side MOSFETs in each half bridge. They are asserted high, meaning a logic "1" will turn on the high side. These are CMOS logic levels. There are no provisions for simultaneous conduction lockout or dead time, so high side and low side timing issues need to be accommodated outside this module. For a logic "1" to maintain the high side MOSFET ON condition, sufficient voltage needs to be stored on the VB capacitors. Because there are no high side power supplies, the voltage to the VB capacitors are "bootstrap charged" to the VCC supply when the low side MOSFET is turned ON. There is limited charge in these capacitors , and the charge will be depleted as the high side stays ON for extended amounts of time. For extended high side ON conditions, use larger VB capacitors.

ALO, BLO, CLO, DLO - Are the logic pins for controlling the low side MOSFETs in each half bridge. They are asserted high, meaning a logic "1" will turn on the low side. These are CMOS logic levels. There are no provisions for simultaneous conduction lockout or dead time, so low side and high side timing issues need to be accommodated outside this module.

SD - Is the pin for shutting down the complete module. It is logic level, with a logic "1" disabling all of the half bridges. The input is CMOS.

AVB+, BVB+, CVB+, DVB+ - Are the pins for the positive side of the external bootstrap capacitor. The sizing of this capacitor dictates how long the high side MOSFETs can stay on before needing refresh or will turn off due to lack of voltage.

AVB-, BVB-, CVB-, DVB- - Are the pins for the negative side of the external bootstrap capacitor.

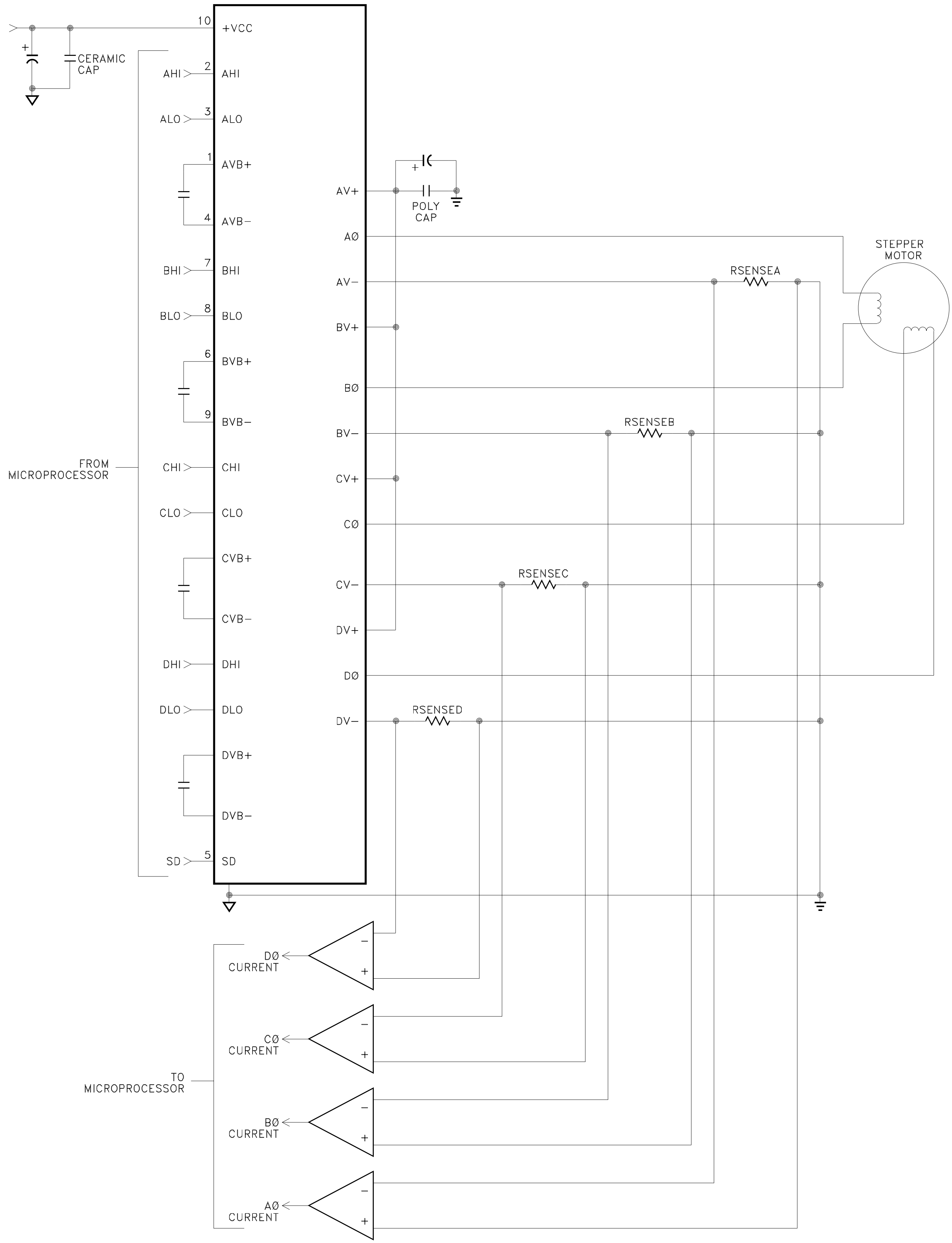
VCC - Input power connection for the bias supply. A 22uF capacitor and a 0.1uF capacitor are recommended between this pin and GND, as close to the module as possible.

GND - Return pin for the input bias supply power. The bypass capacitors shall be connected to this pin as close to the module as possible. An input ground plane is recommended, so as to keep stray inductance down to a minimum. Since this is a non-isolated device between input power and output power, there needs to be a connection between GND and the return of the output stage power. The recommended two ground planes shall connect together at one point, this GND pin, with a 0.100" width trace of minimum length. This will minimize sharing ground currents that will tend to move the input ground around and pass transient noise to the input.

TOTAL DOSE RADIATION AND SEE TEST PERFORMANCE

Radiation performance curves for TID testing will be generated for all radiation testing performed by MSK. These curves show performance trends throughout the TID test process and are located in the MSK4231RH radiation test report. The complete radiation test report will be available in the RAD HARD PRODUCTS section on the MSK website. Contact MSK for SEE test results.

TYPICAL APPLICATION CIRCUIT



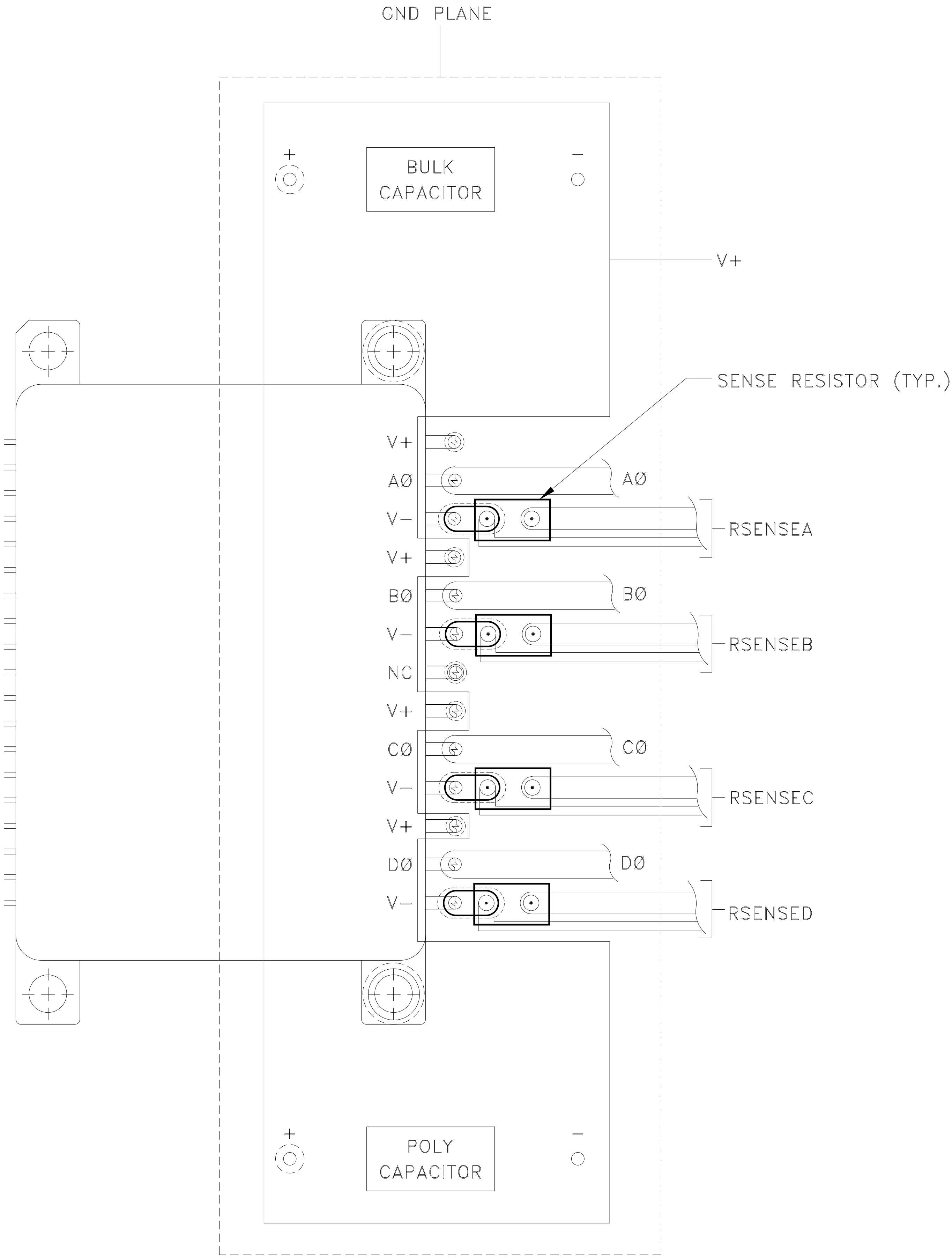
TYPICAL APPLICATION LAYOUT

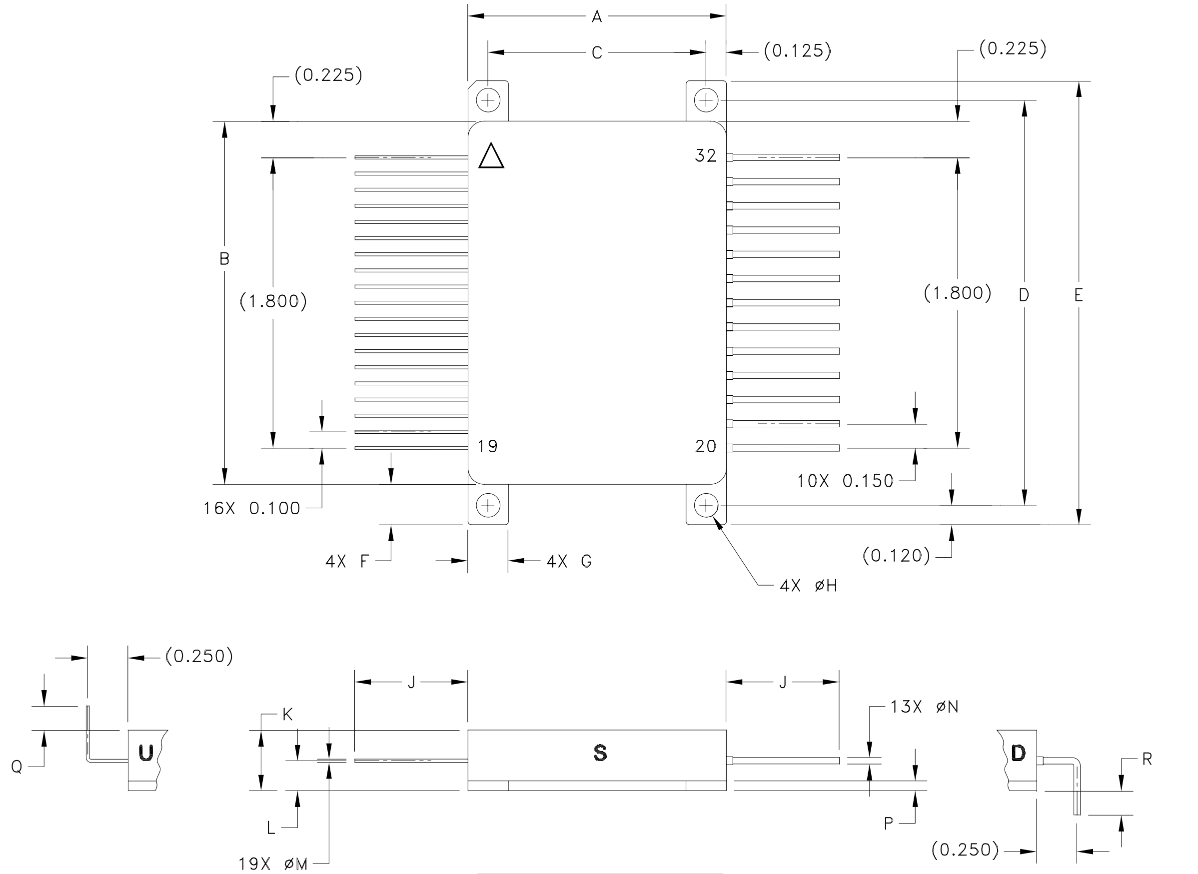
Shown is a typical application with the output stage PC board layout using sense resistors for the 4 half bridge legs. There are 2 planes, one for the V+ power input, and one for the Ground return. They are to be on separate layers. The typical placement of the 2 types of capacitors are also shown. V+ power and Ground return should connect to the same end of the PC board assembly, such that output currents between the V+ and the Ground will cancel if they are flowing in the opposite direction, minimizing inductance.

The 2 planes shall be as wide as possible to minimize stray inductance. With the 2 types of capacitors split with the module in the middle, it tends to again minimize stray inductance between it and the capacitances. It may be desirable to split both the bulk capacitance and the poly capacitance and place one of each on each end of the module to further spread the capacitance out and minimize the effect of stray inductance.

With the sense resistors and their connections shown, it is important to minimize trace length and keep the widths as wide as possible for inductance reasons. The sense resistors shall be non-inductive, and have heatsinking appropriate to the value of resistor selected. The sense traces do not carry significant current, so they can be routed back to the sensing and amplification circuitry elsewhere. It is important to keep the sense and return traces for each resistor routed in close proximity to minimize noise pickup and capitalize on the common mode rejection of a typical differential amplifier input.

This example of a layout is a typical one only. It is not intended to conform to any layout standards, but to show the concept of the layout, current flow, and the use of planes for power and return.


GND PLANE
BULK
CAPACITOR
+
−
V+
SENSE RESISTOR (TYP.)
V+
AØ
V−
V+
BØ
V−
NC
V+
CØ
V−
V+
DØ
V−
AØ
RSENSEA
BØ
RSENSEB
CØ
RSENSEC
DØ
RSENSED
POLY
CAPACITOR
+
−



REF	MIN	MAX
A	1.590	1.610
B	2.240	2.260
C	1.340	1.360
D	2.500	2.520
E	2.740	2.760
F	0.245	0.255
G	0.245	0.255
H	0.142	0.149
J	0.600	———
K	———	0.395
L	0.175	0.195
M	0.017	0.023
N	0.037	0.043
P	0.055	0.065
Q	0.120	———
R	0.120	———

ESD TRIANGLE INDICATES PIN 1
WEIGHT=70 GRAMS TYPICAL

ALL DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

MSK4231 K RH U

LEAD CONFIGURATION
S=STRAIGHT, U=BENT UP, D=BENT DOWN

RADIATION HARDENED

SCREENING
BLANK=INDUSTRIAL; H=MIL-PRF-38534 CLASS H;
K=MIL-PRF-38534 CLASS K

GENERAL PART NUMBER

REVISION HISTORY

REV	STATUS	DATE	DESCRIPTION
A	Released	02/15	Initial Release

MSK

www.anaren.com/msk