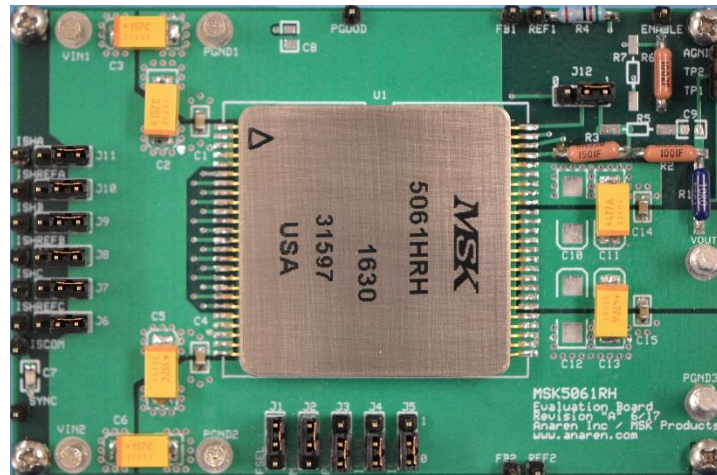# MSK5061RH
Evaluation Board User's Guide
REV A, 8-02-17

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Introduction

The MSK5061RH is a Radiation Hardened adjustable-output switching regulator featuring support for current sharing operation. The MSK5061RH integrates a radiation hardened current mode buck regulator IC, output inductor, and many supporting passive components in a compact hermetic 50-pin flatpack. A full suite of features simplifies development of sophisticated and rugged point of load power supplies for demanding loads such as FPGAs, ASICS, and Microprocessors.

The MSK5061RH Evaluation Board provides a platform from which to evaluate performance and experiment with design changes for your application. Excessive ripple, instability, and other costly technical problems in flight hardware can be avoided with evaluation early in the design cycle.

This application note is intended to be used in conjunction with the MSK5061RH data sheet. Reference the MSK5061RH data sheet for additional application information and specifications.

Evaluation Board Setup (Single Board Operation)

The MSK5061RH Evaluation Board is jumper configurable to operate either independently or in Current Share mode with a second evaluation board for increased load current capacity. Switching Frequency, Power On Reset threshold, and SYNC pin function are also jumper configurable.

The factory default configuration is for single board operation. Jumpers J1, J2, J6-J12 shall be in position one, J3-J5 shall be in position 0. Refer to Single Board Schematic in Figure 12. The default configuration shall have the following operation characteristics; VOUT = 1.0V for 3.3 ≥ Vin ≤ 5.0V and 0A ≥ Load Current ≤ 10A. Switching Frequency = 1MHz. The Power On Reset threshold is approximately 2.8V.

Use the turret terminals to connect to your test equipment. Connect a 3V to 5.5V power supply to VIN1 and PGND1 terminals. Connect the load the VOUT and PGND3 terminals.

Connect measurement equipment using Kelvin Sensing techniques to ensure accurate load regulation and efficiency measurements. TP1/AGND is the recommend test points for measuring VOUT. The ground wire from an oscilloscope probe acts as an antenna picking up radiated EM fields making waveforms such as output ripple voltage appear noisy. For improved VOUT Ripple Voltage Waveforms use a probe ground spring clip of minimal length and probe directly across C15.

Evaluation Board Setup (Current Share Operation)

Two MSK5061RH Evaluation Boards are required to demonstrate Current Share operation. One board is configured as the Current Share Master and the other board is configured as the Current Share Slave. See table 1 for Master board and Slave board jumper positions and component value changes.

	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	C8
Master	0	1	0	1	0	0	0	0	0	0	0	*Note	N.P.
Slave	0	0	0	1	1	0	0	0	0	0	0	0	0.1uF

Note: Short together all three terminals of J12
Table 1

Using short jumper wires connect the following terminals on the Master board to the corresponding terminals on the Slave board; ISHA, ISHREFA, ISHB, ISHREFB, ISHC, ISHREFC, ISHCOM, PGOOD, SYNC, FB, REF.

Similarly connect the VINx, PGNDx, VOUT and PGND3 terminals using conductors sized appropriately for the anticipated operating currents. Care should be taken to symmetrically distribute the parasitic conductor resistance between the Master, Slave and Load to approach ideal current sharing performance. Reference the photograph in figure 1 below for an example of the required connections

The Current Share Operation configuration shall have the following operation characteristics; VOUT = 1.0V for 3.3 ≥ Vin ≤ 5.0V and 0A ≥ Load Current ≤ 18A. Switching Frequency = 500kHz. The Power On Reset threshold is ≈2.8V.

Figure 1, Current Share Connections

ENABLE Pin Function

R6 is populated with a 10KΩ resistor pulling the ENABLE pin up to VIN. The MSK5061RH will begin its Soft-Start cycle and VOUT will rise into regulation as soon as VIN exceeds the Power On Reset Threshold selected by J3.

R7 can be populated to provide a different turn on threshold and hysteresis. Refer to the MSK5061RH data sheet for more detailed information.

SS Pin Function

The MSK5061RH Evaluation Board Soft-Start time can be increased upto 240mS by installing capacitor C8. Increasing the soft start time decreases startup input surge current. Note: for current share operation, the slave's soft start time should be at least twice that of the master's. Reference the MSK5061RH data sheet for governing equations.

REF Pin Function

The 0.6V precision reference voltage for the PWM error amplifier is brought out to the REF pin to facilitate current share operation only. The REF pin must remain otherwise unloaded.

M/S and SYNC Pin Functions

The MSK5061RH SYNC pin function is determined by the level on the M/S pin. If M/S is high, the SYNC pin is a clock output in phase with the PWM oscillator. If the M/S is low the SYNC pin will accept and synchronize switching to an external clock signal. Jumper J2 on the evaluation board connect M/S to either VIN (position 1) or PGND (position 0).

Output Voltage Programming

The VOUT voltage is determined by the R2-R3 divider network connected between VOUT, FB and AGND.

$$VOUT = V_{REF} \times \left(\frac{R2}{R3} + 1\right) \longrightarrow R3 = \frac{R_2 \times V_{REF}}{VOUT - V_{REF}}$$

Given: V_{REF} = 0.6V and R2 = 1kΩ
VOUT = 1.0V, R3 = 1.5kΩ
VOUT = 1.8V R3 = 500Ω
VOUT = 2.5V, R3 = 316Ω
VOUT = 3.3V, R3 = 222Ω

Input Capacitors

Buck topology switching regulators such as the MSK5061RH draw current from the input bus in trapezoidal pulses with fast edges. Ceramic capacitors integrated inside the MSK5061RH provide a low impedance source for the high frequency content of the input current waveform. Bulk (tantalum) capacitance and additional ceramic capacitors located close to the MSK5061RH are required to control input ripple voltage and ripple current stresses. The MSK5061RH Evaluation Board uses AVX TBM series 150uF 16V tantalum input capacitors. These were selected to provide a generic starting point using high reliability components. See the BOM for specific part numbers. The value and type of bulk input capacitors should be optimized for your particular application based on worst-case operating conditions and derating requirements.

Output Capacitor Selection

The output capacitors C11 and C13 are AVX TBM series 470uF tantalum capacitors. The value of the output capacitors and their parasitic elements determine several important performance characteristics of a switching regulator such as stability margins, loop bandwidth, load step response, output ripple voltage, start-up surge current, and output response to Single Event Transients.

The output ripple voltage is determined by the inductor ripple current and output capacitor ESR. Lower output ripple voltage can be obtained by selecting a lower ESR capacitor or placing more capacitors in parallel. For very low ripple, an additional LC filter added to the output may be a more suitable solution. Loop stability margins must be re-evaluated if the output capacitance is altered. The output contains narrow voltage spikes caused by the parasitic inductance of C11 and C13. Ceramic capacitors C14 and C15 help absorb these spikes on the demo board. In application, distributed trace impedance and local bypass capacitors will help serve this function.

With current mode control, the output stage pole is established by the load impedance and output capacitance. ESR of the bulk output capacitance forms and zero and can help improve phase margin. Ceramic capacitors with equivalent bulk have comparatively negligible ESR. The impact on loop dynamics should be considered if using large values of ceramic capacitors. The Evaluation Boards are designed to provide good stability margins over a broad range of applications and conditions. There is no one size fits all solution; analysis and experimental verification will ensure performance and high reliability.

The MSK5061RH Evaluation Board is designed to facilitate a common stability measurement technique. Use an isolation transformer to inject the output of a Network Analyzer into the control loop across R1 (terminals TP1 and TP2). Connect the inputs of the analyzer to TP1(loop output) and TP2(loop input). Use the AGND terminal as the ground reference for the network analyzer inputs. The analyzer will inject a frequency swept sinewave signal into the control loop, and plot the system gain and phase response. Figures 2 and 3 illustrates typical results for single board operation. Figures 4 and 5 illustrate typical results for Current Sharing operation. R5 and C9 are not populated by default but can be used to modify loop dynamics.
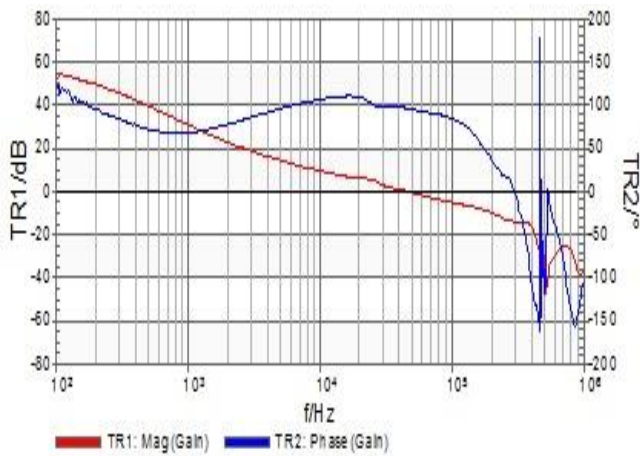
Figure 2, Single Board Vin = 1V, Vout = 3.3V, 0A
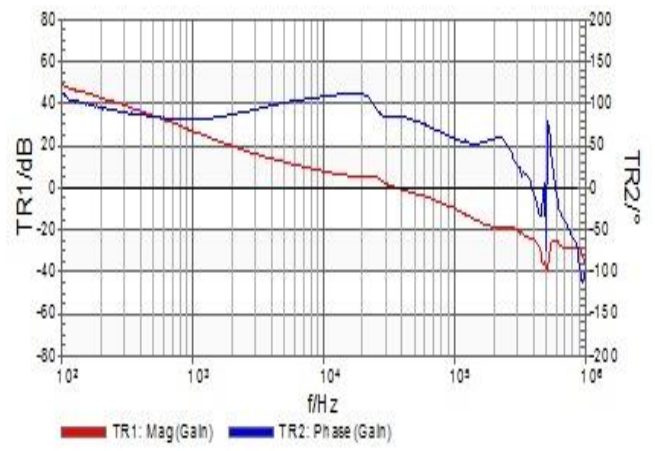
Figure 3, Single Board Vin = 1V, Vout = 3.3V, 8A
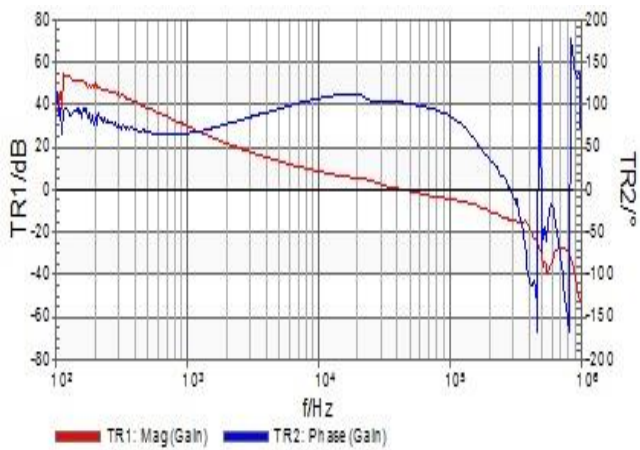
Figure 4, Current Sharing; Vin = 1V, Vout = 3.3V, 0A
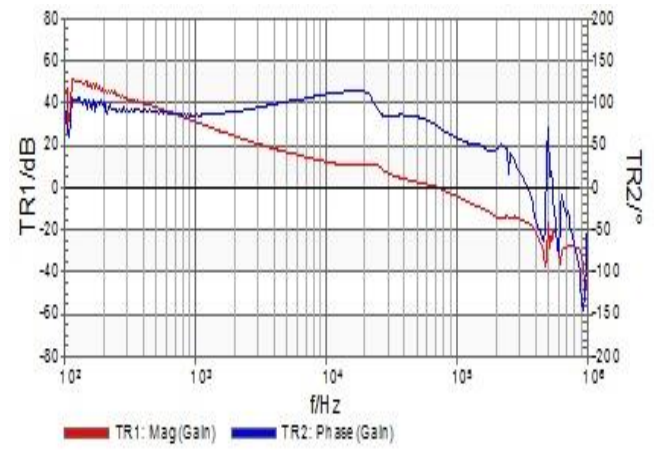
Figure 5, Current Sharing Vin = 1V, Vout = 3.3V, 16A

Single Board Operation

Parameter	Conditions	Units	Typical
Output Voltage	IL = 5A, VIN = 3.3V	V	1.0
Switching Frequency	IL = 5A, VIN = 3.3V	MHz	1.0
Output Ripple Voltage	IL = 10A, VIN = 3.3V	mVpp	8
Line Regulation	IL = 5A, 3V ≤ VIN ≤ 5.5V	%	0.1
Load Regulation	IL = 0A to 10A, VIN = 3.3V	%	-0.1
Efficiency	IL = 5A, VIN = 3.3V	%	76.4
Current Limit	VIN = 5V	A	11.5
Gain Margin	IL = 8A, VIN = 3.3V	dB	24
Phase Margin	IL = 8A, VIN = 3.3V	Deg	85

Figure 6, Single Board Load Step 1A to 8A
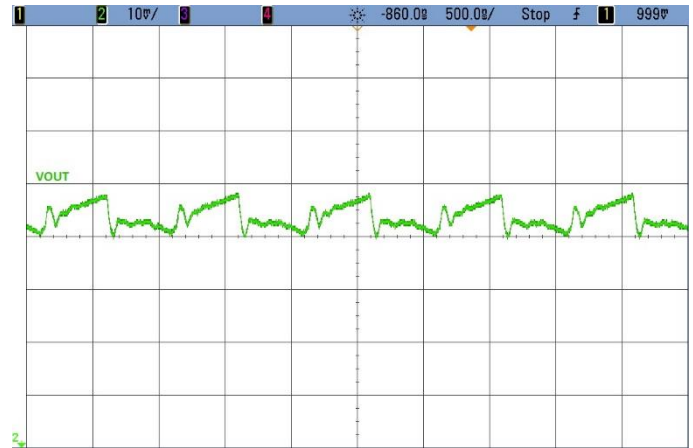
Figure 7, Single Board Output Ripple Voltage
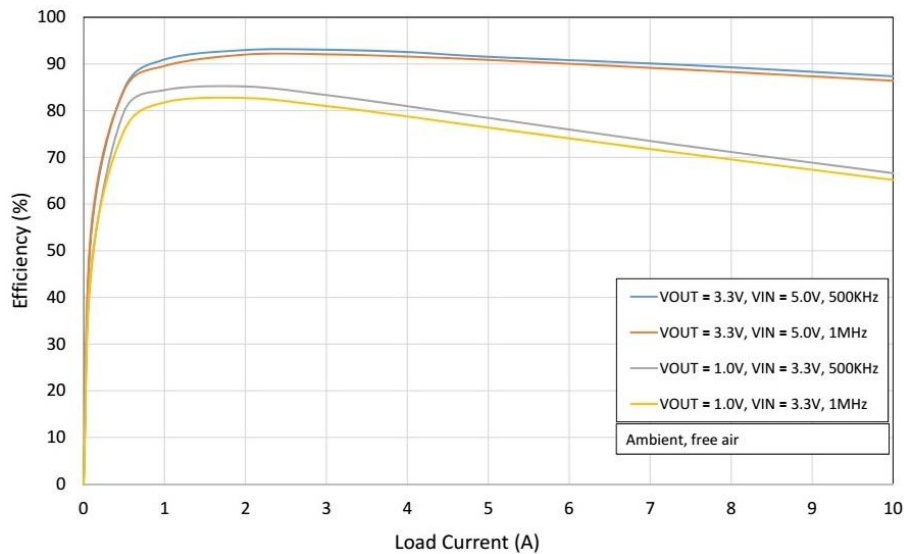
Figure 8, Single Board Efficiency

Current Share Operation

Parameter	Conditions	Units	Typical
Output Voltage	IL = 10A, VIN = 3.3V	V	1.0
Switching Frequency	IL = 10A, VIN = 3.3V	KHz	500
Output Ripple Voltage	IL = 10A, VIN = 3.3V	mVpp	5
Line Regulation	IL = 10A, 3V ≤ VIN ≤ 5.5V	%	0.1
Load Regulation	IL = 0A to 16A, VIN = 3.3V	%	-0.2
Current Share Ratio	IL = 10A, VIN = 3.3V, Io_{slave} / Io_{master}	-	1.18
Efficiency	IL = 16A, VIN = 3.3V	%	70
Current Limit	VIN = 3.3V	A	19
Gain Margin	IL = 16A, VIN = 3.3V	dB	16.8
Phase Margin	IL = 16A, VIN = 3.3V	Deg	71.2
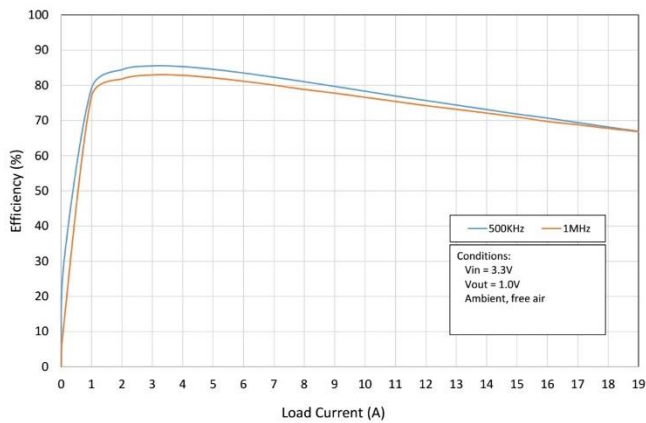
Figure 9, Current Share Operation Efficiency
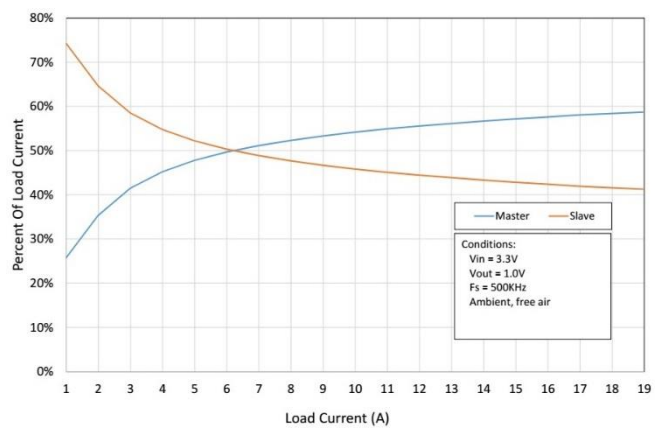
Figure 10, Current Sharing Performance
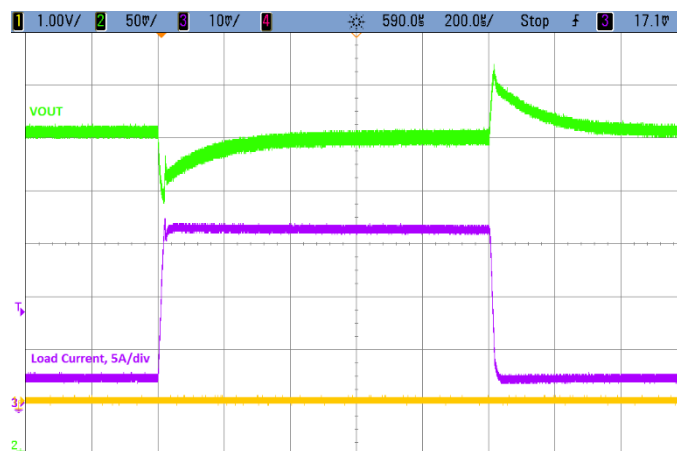
Figure 11, Current Share Operation Load Step Response, 2A to 16A
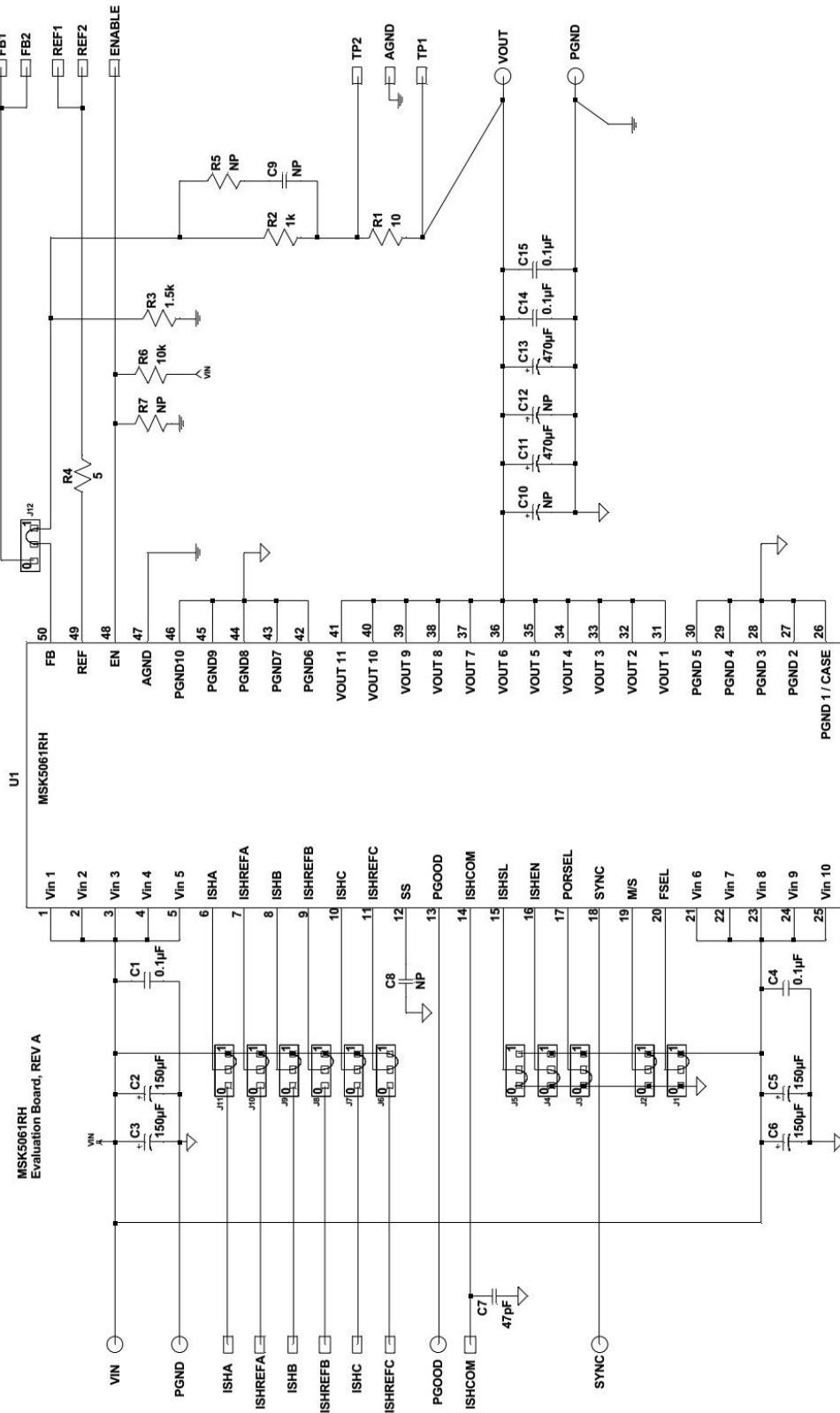
Figure 12, Single Board Operation Schematic
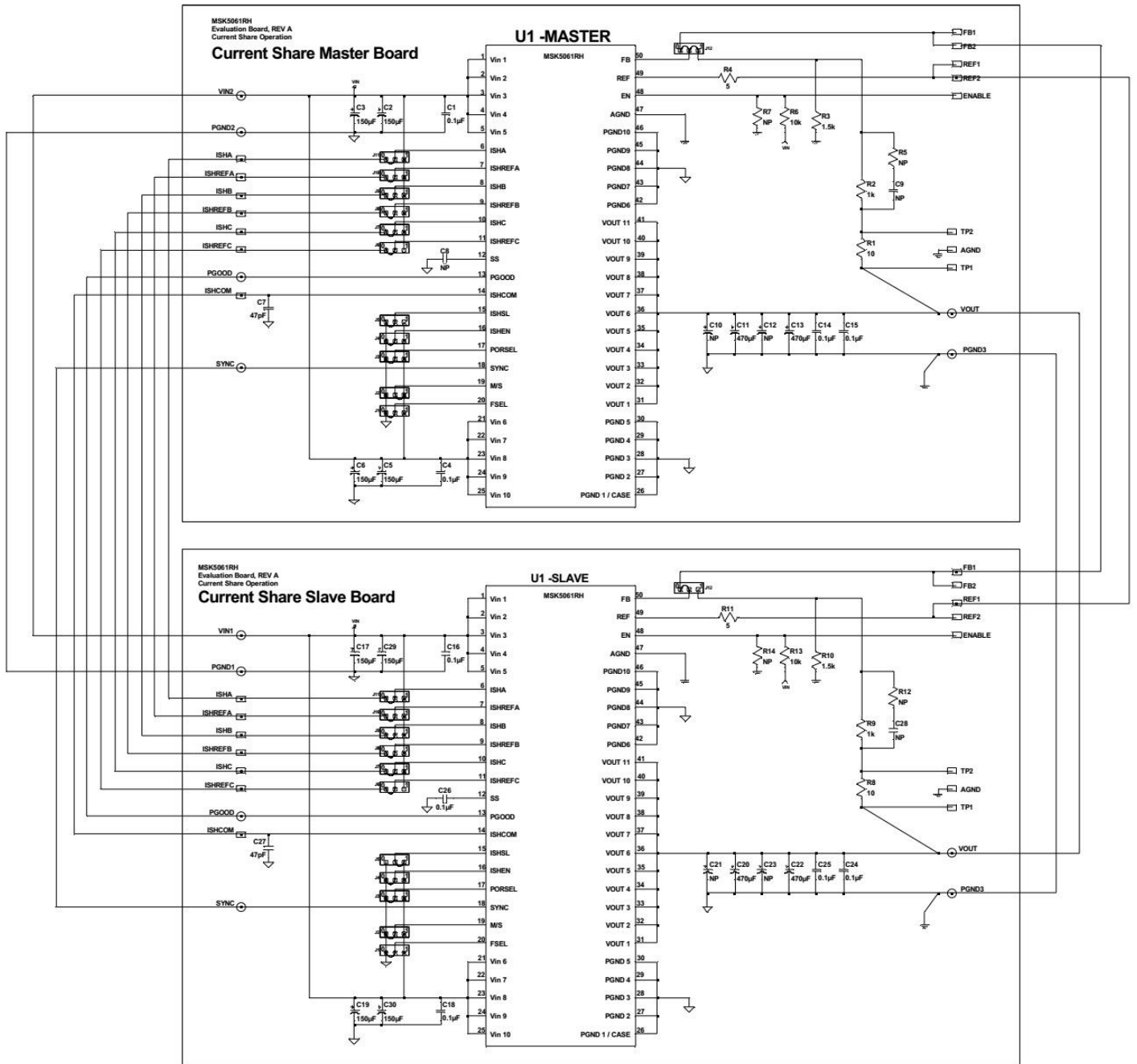
Figure 13, Current Share Operation Schematic
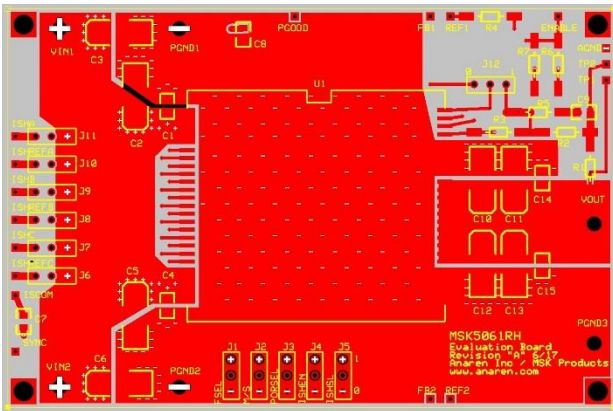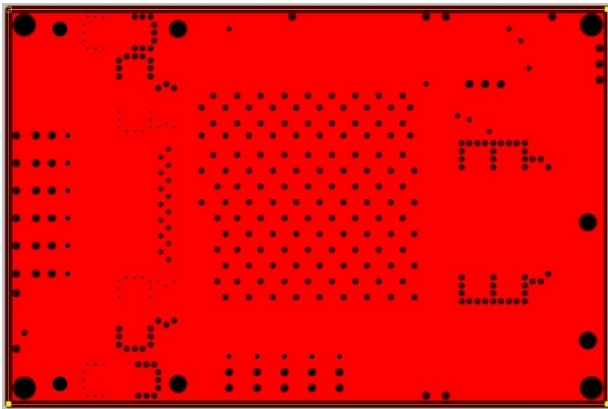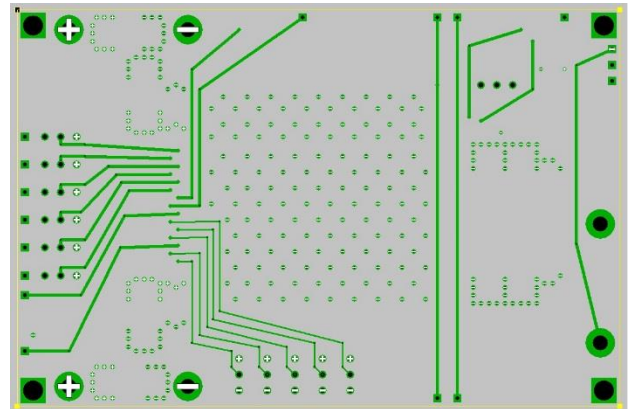
Layer 1, Power and Signal
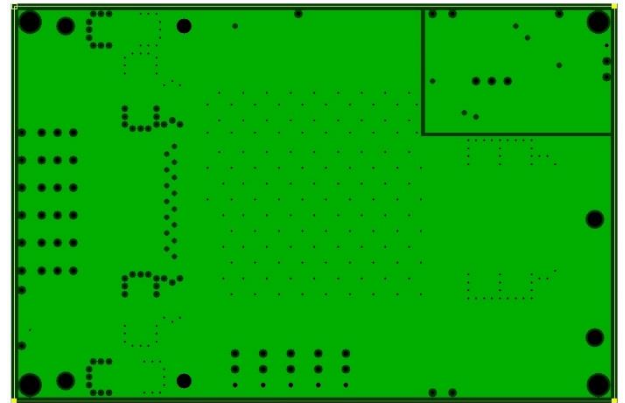
Layer 2, PGND and AGND planes

Layer 3, VIN plane

Layer 4, Signal

Layout Considerations

The FB pin is a high impedance node and is susceptible to noise pickup. Use minimal trace lengths to R1 and R2 and avoid routing near switching nodes or shield with a low impedance plane layer.

Orient the ceramic capacitors connected to VIN and PGND to provide the smallest possible current loop area. Mount the output capacitors symmetrically between VOUT, PGND pins 26-30 and PGND pins 42 -46. Pin 26 connects to both the internal power ground node and the case. This case connection is not designed to conduct heavy load return currents. Use heavy copper planes to provide a low resistance return path from the load to the input source.

Symmetrically distribute the parasitic conductor resistance between the Master, Slave, and Load to ensure optimal current sharing.

Ref Des	Description	Manufacturer	Part Number
U1	Rad Hard Low Voltage 10A Switching Regulator With Current Share	Anaren, Inc. – MSK Products	MSK5061RHG
C1, 4, 14, 15	0.1uF, 10%, 100V, X7R, 8050	AVX	08053C104K
C2, 3, 5, 6	150UF, 10%, 16V, Tantalum	AVX	TBME157K016L
C7	47pF, 10%, 100V, NPO, 8050		
C8	NP - Not Populated (Slave Board ≥ 0.1µF)		
C9	NP - Not Populated		
C10, 12	NP - Not Populated		
C11, 13	470uF, 10%, 10V, Tantalum	AVX	TBME477K010L
R1	10Ω, 1%, 1/8W, RNC		
R2	1kΩ, 1%, 1/8W, RNC		
R3	1.5kΩ, 1%, 1/8W, RNC		
R4	5Ω, 1%, 1/8W, RNC		
R5	0Ω, 1%, 1/8W, RNC		
R6	10kΩ, 1%, 1/8W, RNC		
R7	NP		

Notes: