MIL-PRF-38534 & 38535 CERTIFIED FACILITY

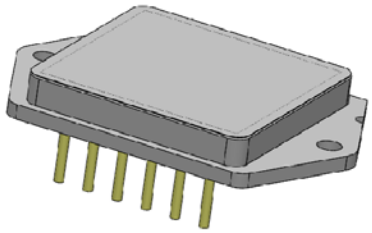
M.S.KENNEDY CORP.

100 VOLT 30 AMP H-BRIDGE PWM MOTOR DRIVER/AMPLIFIER

4205

FEATURES:

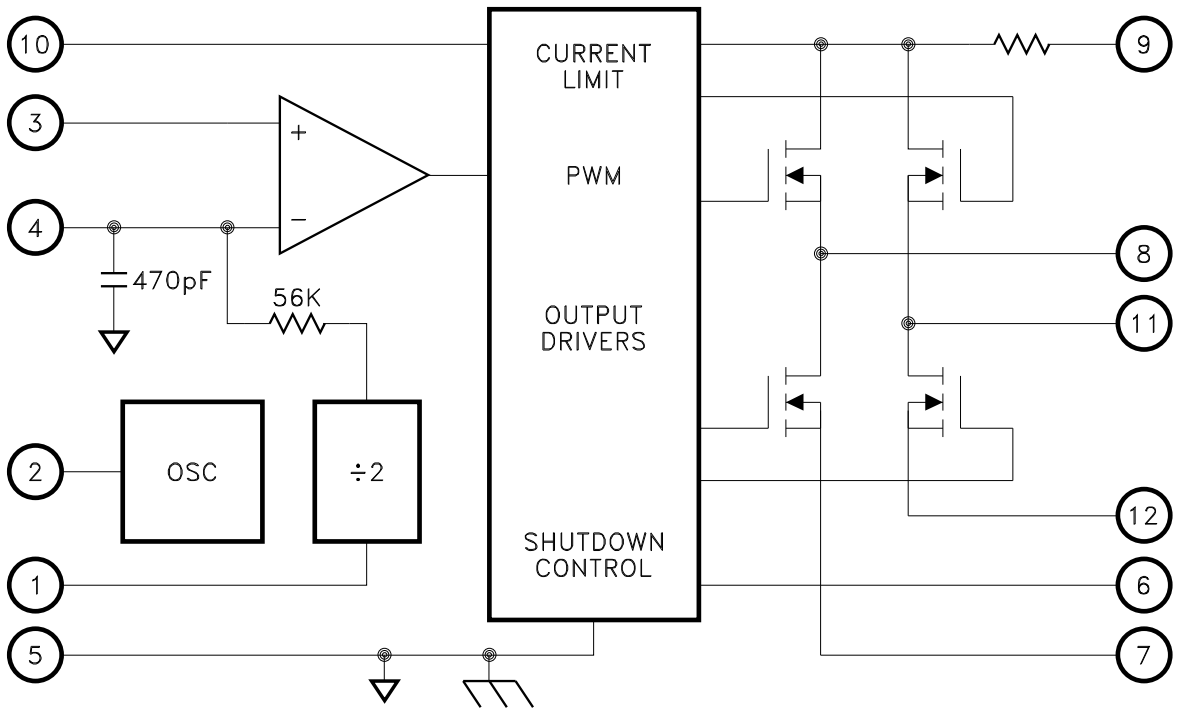
- New TUB Version Replaces the Platform Package
- Replaces APEX SA03 PWM Amplifier
- 100 Volt, 30 Amp Capability
- Self-Contained Smart Lowside/Highside Drive Circuitry
- Internal PWM Generation, Shoot-through Protection
- Grounded Case Allows Direct Heatsinking
- Available Fully Screened To MIL-PRF-38534 Class H
- Contact MSK for MIL-PRF-38534 Qualification Status



DESCRIPTION:

The MSK4205 is a complete H-Bridge microcircuit intended for use in DC brushed motor control application or Class D switchmode amplification in severe operating conditions. The MSK4205 can be used as a drop in replacement for the APEX SA03 in applications that do not utilize the thermal limit feature. All of the drive/control circuitry for the lowside and highside are internal to the device. The clock input stage divides the internal oscillator frequency by two, which provides the switching frequency of 22.5KHz. An external oscillator may be used to lower the frequency or synchronize multiple amplifiers. Current sensing is provided for each half of the bridge and fixed highside current limit is provided internally. Lowside current limit is user controlled with the use of an external resistor network. An internal highside charge pump allows 100% duty cycle. The design is packaged in a hermetic 12 pin bolt down power TUB package.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- MOTOR CONTROL
- REACTIVE LOADS
- PIEZO ELEMENTS

PIN-OUT INFORMATION

1	CLK IN	7	ISENSE B
2	CLK OUT	8	B OUT
3	+PWM	9	+VS
4	-PWM/RAMP	10	+VCC
5	GND/CASE	11	A OUT
6	ILIM/SHDN	12	ISENSE A

8548-53 Rev. H 6/14

ABSOLUTE MAXIMUM RATINGS ⑪

+V	High Voltage Supply	100V
+VCC	Logic Supply	16V
IOUT	Continuous Output Current	30A
IPK	Peak Output Current	40A
VOUT	Output Voltage Range	GND to V+ max.
VIN	Input Voltage, +PWM and -PWM	0V to 11V
VL	Logic Input Voltage (ILIM/SHDN)	0V to 10V

TST	Storage Temperature Range ⑫	-65°C to +150°C
TLD	Lead Temperature Range (10 Seconds)	300°C
TC	Case Operating Temperature Range	
	MSK4205H	-55°C to +125°C
	MSK4205	-40°C to +85°C
TJ	Junction Temperature	+150°C
θJc	Thermal Resistance	
	(Output FETS @ 125°C)	0.75°C/W
	(Output FETS @ 25°C)	0.65°C/W

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions	Group A Subgroup	MSK4205H Min.	MSK4205H Typ.	MSK4205H Max.	MSK4205 Min.	MSK4205 Typ.	MSK4205 Max.	Units
OUTPUT CHARACTERISTICS									
VDS(ON) Highside	ID = 10A	1	-	0.60	1.0	-	0.60	1.2	V
		2	-	0.85	1.3	-	0.85	-	V
		3	-	0.38	0.7	-	0.38	-	V
VDS(ON) Lowside	ID = 10A	1	-	0.46	0.8	-	0.46	1.0	V
		2	-	0.65	1.0	-	0.65	-	V
		3	-	0.25	0.5	-	0.25	-	V
VDS(ON) Highside ② ⑦	ID = 30A	1	-	1.45	-	-	1.45	-	V
		2	-	2.20	-	-	2.20	-	V
		3	-	0.86	-	-	0.86	-	V
VDS(ON) Lowside ② ⑦	ID = 30A	1	-	0.97	-	-	0.97	-	V
		2	-	1.65	-	-	1.65	-	V
		3	-	0.45	-	-	0.45	-	V
Forward Voltage (Body Diode) Highside ②	ID = 10A	1	-	1.15	-	-	1.15	-	V
		2	-	0.97	-	-	0.97	-	V
		3	-	1.20	-	-	1.20	-	V
Forward Voltage (Body Diode) Lowside ②	ID = 10A	1	-	0.95	-	-	0.95	-	V
		2	-	0.78	-	-	0.78	-	V
		3	-	1.0	-	-	1.0	-	V
Forward Voltage (Body Diode) Highside ② ⑦	ID = 30A	1	-	1.70	-	-	1.70	-	V
		2	-	1.72	-	-	1.72	-	V
		3	-	1.68	-	-	1.68	-	V
Forward Voltage (Body Diode) Lowside ② ⑦	ID = 30A	1	-	1.28	-	-	1.28	-	V
		2	-	1.26	-	-	1.26	-	V
		3	-	1.29	-	-	1.29	-	V
RDS(ON) each MOSFET ② ⑥		1	-	30	55	-	30	55	mΩ
		2	-	60	-	-	60	-	mΩ
Leakage Current, Highside ⑧	+VS = 80V	1, 2	-	2.0	3.0	-	2.0	3.0	mA
Leakage Current, Lowside ⑨		1, 2	-	4.0	6.0	-	4.0	6.0	mA
OUTPUT FREQUENCY and DUTY CYCLE									
Switching Frequency	Internal Osc ÷ 2	4	22	22.5	23	21	22.5	24	KHz
Duty Cycle	+PWM = 5V	4,5,6	40	50	60	40	50	60	%
	+PWM = 8V, Output A = 100%, Output B = 0%	7	-	Verify	-	-	Verify	-	P/F
	+PWM = 0V, Output A = 0%, Output B = 100%	7	-	Verify	-	-	Verify	-	P/F
SUPPLY CURRENT CHARACTERISTICS									
+VS ② ⑩		1	16	60	100	16	60	100	V
+VCC ②		1	14	15	16	14	15	16	V
+VCC Current	ILIM/SHDN = <90mV	1	-	34	80	-	34	80	mA
+VCC Current	ILIM/SHDN = >110mV	1	-	28	50	-	28	50	mA
+VS	No Load	1	-	10	50	-	10	50	mA
CLOCK CHARACTERISTICS									
Clock Out High Level	IOUT < 1mA	4	4.5	-	5.5	4.5	-	5.5	V
Clock Out Low Level	IOUT < 1mA	4	0	-	0.4	0	-	0.4	V
Frequency		4	44	45	46	42	45	48	KHz
Ramp Center Voltage ②		-	-	5	-	-	5	-	V
Ramp P-P Voltage ②		-	-	4	-	-	4	-	V
CLK IN Low Level ②		1	0	-	0.9	0	-	0.9	V
CLK IN High Level ②		1	3.7	-	5.5	3.7	-	5.5	V
ILIM/SHDN									
Trip Point		1	90	100	110	85	100	115	mV
Input Current ②		1	-	-	100	-	-	100	nA

Reference notes on the following page.

NOTES:

① +VCC = 15V, +VS = 60V, ISENSE A and ISENSE B = Ground, ILIM/SHDN = OV unless otherwise specified.
② Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
③ Class H devices are 100% tested to subgroups 1,2,3,4, and 7. Subgroup 5 and 6 testing available upon request.
④ Subgroup 1,4,7 $T_A = T_C = +25°C$
2,5 $T_A = T_C = +125°C$
3,6 $T_A = T_C = -55°C$
⑤ Industrial grade devices shall be 100% tested at 25°C only.
⑥ The internal on resistance is for the die only. This should be used for thermal calculations only.
⑦ Measured with a constant junction temperature, using a 500μS pulse.
⑧ Includes highside current limit sense bias current.
⑨ Includes bootstrap capacitor charge pump bias current
⑩ If 100% duty cycle is not required +VS min = 0V.
⑪ Continuous operation at or above absolute maximum ratings may adversely effect the device performance and/or life cycle.
⑫ Internal solder reflow temperature is 180°C, do not exceed.

APPLICATION NOTES

MSK4205 PIN DESCRIPTIONS

+VCC - Is the low voltage supply for powering internal logic and drivers for the lowside and highside MOSFETS. The supplies for the highside drivers are derived from this voltage. Optimum operation occurs with +VCC set at 15V.

+VS - Is the high voltage H-bridge supply pin. The MOSFETS obtain the drive current from this supply pin. The MOSFETS are rated at 100 volts. Proper bypassing to GND with sufficient capacitance to suppress any voltage transients, and ensure removal of any drooping during switching, should be done as close to the pins on the hybrid as possible.

AOUT - Is the output pin for one half of the bridge. Increasing the +PWM voltage causes increasing duty cycles at this output.

BOUT - Is the output pin for the other half of the bridge. Decreasing the +PWM voltage causes increasing duty cycles at this output.

ISENSE A - Is the connection for the bottom of the A half bridge. Connect a sense resistor between ISENSE A and +VS return ground for current limit sensing, or connect directly to ground if current sense is not desired. The maximum voltage on these pins is ±5 volts with respect to GND.

ISENSE B - Is the connection for the bottom of the B half bridge. Connect a sense resistor between ISENSE B and +VS return ground for current limit sensing, or connect directly to ground if current sense is not desired. The maximum voltage on these pins is ±5 volts with respect to GND.

GND - Is the return connection for the input logic and +VCC. This pin is also connected to the package case. No current shall be allowed to flow in the case.

+PWM - Is an analog input for controlling the PWM pulse width of the bridge. A voltage higher than 5V will produce greater than 50% duty cycle pulses out of A OUT. A voltage lower than 5V will produce greater than 50% duty cycle pulses out of B OUT.

ILIM/SHDN - Is the connection for disabling all 4 output switches. SHUTDOWN high overrides all other inputs. When taken low, everything functions normally. This pin should be grounded if not used.

APPLICATION NOTES CONT'D

MSK4205 OPERATING CONSIDERATIONS

STARTUP CONDITIONS and UNDER VOLTAGE LOCKOUT

The under voltage lockout function of the MSK4205 prevents the device from starting before sufficient bias voltage is available. The U_{VLO} feature monitors the +VCC supply and holds the outputs low until the voltage level rises above the threshold during start up. After start up the lowside U_{VLO} circuit will hold the lowside switches off if +VCC falls below the threshold. The highside of the all N channel output bridge circuit is driven by bootstrap circuit and charge pump arrangement. The highside U_{VLO} circuit will hold the highside switches off any time the voltage on the bootstrap capacitor falls below the threshold. In order for the bootstrap capacitor to charge above the U_{VLO} the lowside of each half of the bridge circuit must have been previously in the ON state. This means that if the input signal to the MSK4205 at startup is demanding a 100% duty cycle, the output may not follow the command and the highside switches may be in an unknown state. The ramp signal must cross the input signal at some point to correctly determine the output thereafter. +VCC and Bootstrap charge must be greater or equal to 10V to ensure under voltage lockout does not engage. For further duty cycle restriction reference the MAXIMUM DUTY CYCLE section.

MAXIMUM DUTY CYLE

The MSK4205 uses two independent bootstrap circuits and charge pump arrangement to power each of the high side switches. When the switches are turned on the high side drivers are powered by the charge in the bootstrap capacitors. If +VS is 16V or higher the charge pump will maintain the bootstrap charge regardless of the duty cycle. If +VS is less than 16V the voltage on the bootstrap capacitors will have an initial 1.7V drop and decays at a rate of approximately 235mV every 100uS. The voltage can be approximated by the equation:

V_{BS} = +VCC-1.7V-2.35 x T_{ON}
T_{ON} is the switch on time in mS
V_{BS} is the bootstrap capacitor voltage

V_{BS} should be greater or equal to 10 volts to ensure that V_{BS} does not drop below the U_{VLO} threshold. To regenerate the bootstrap charge the lowside switches must be activated every cycle or held active during static operation to provide a return path for charging.

CURRENT LIMIT

There are two load current sensing pins, ISENSE A and ISENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see Figures 1 and 2). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the ISENSE pins. To avoid errors due to lead lengths connect the I_{LIMIT}/S_{HDN} pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the +VS return. Switching noise spikes will invariably be found at the ISENSE pins. The noise spikes could trip the current limit threshold which is only 100mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND pin of the amplifier. Suggested starting values are $C_{FILTER} = 0.01\mu F$, $R_{FILTER} = 5K$. The required value of R_{LIMIT} in voltage mode may be calculated by: $R_{LIMIT} = 0.1V/I_{LIMIT}$ where R_{LIMIT} is the required resistor value and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure 2). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

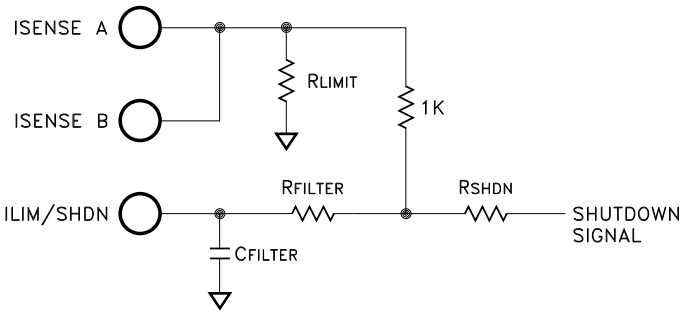


FIGURE 1

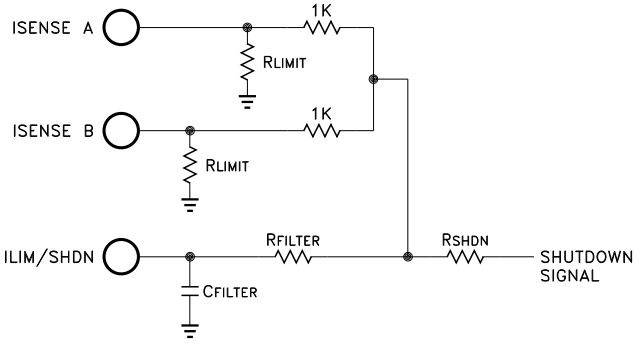


FIGURE 2

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45KHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the -PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 45KHz is chosen an external capacitor must be tied to the -PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

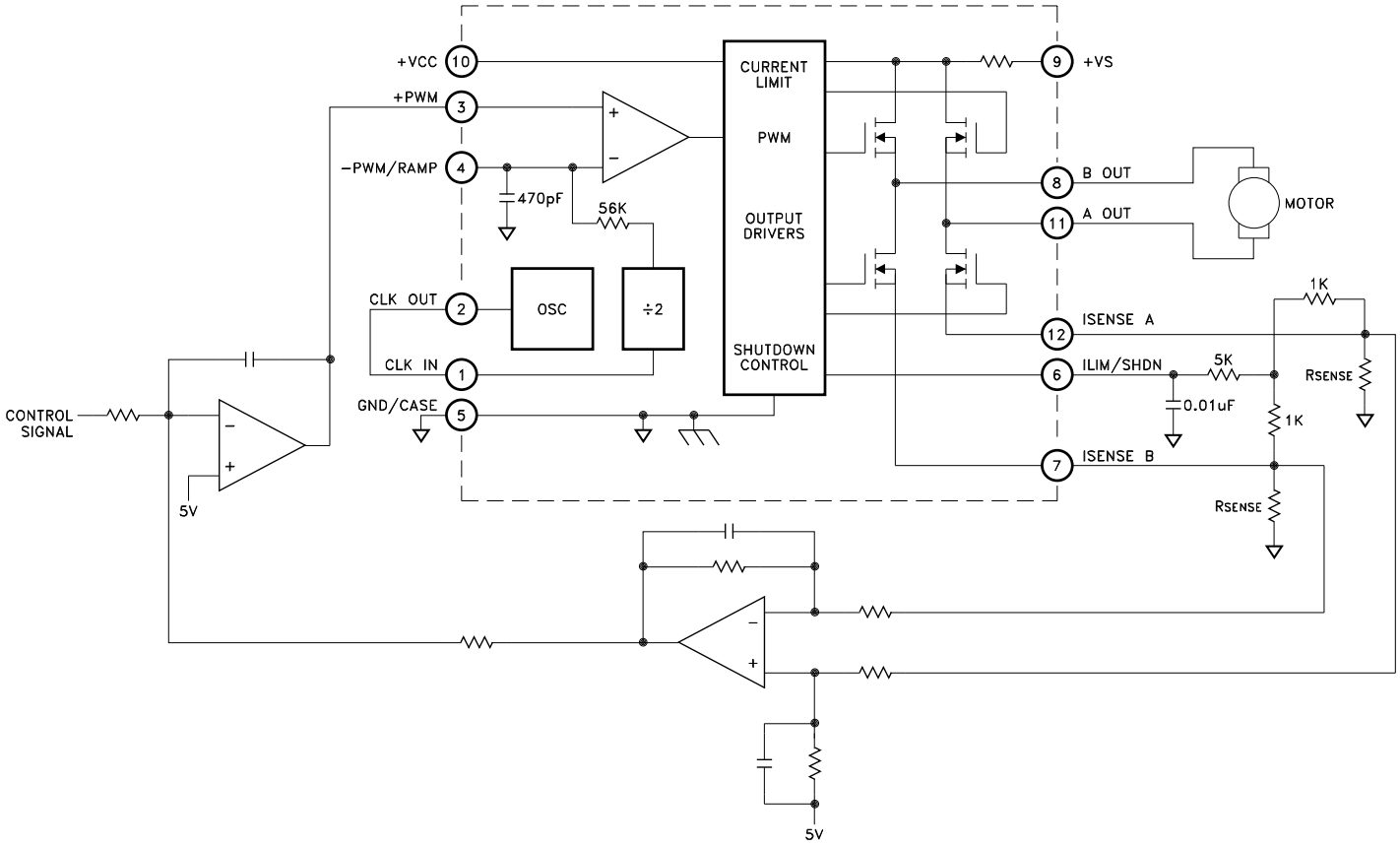
PWM INPUTS

The full bridge driver may be accessed via the pwm input comparator. When +PWM > -PWM/RAMP then AOUT > BOUT. A motion control processor which generates the pwm signal can drive these pins with signals referenced to GND.

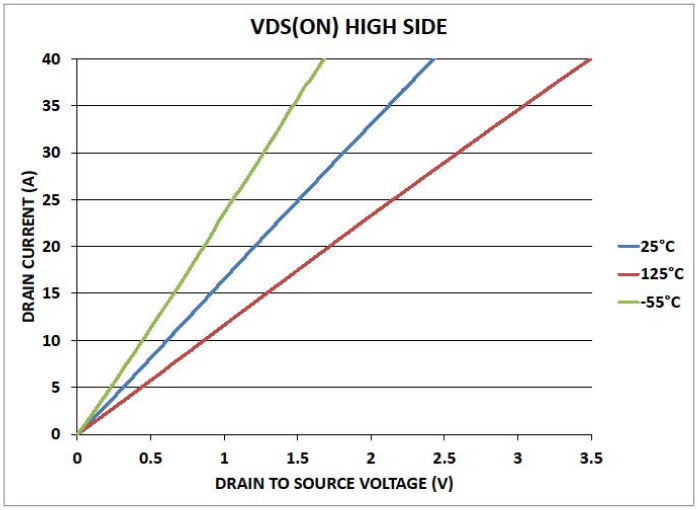
PROTECTION CIRCUITS

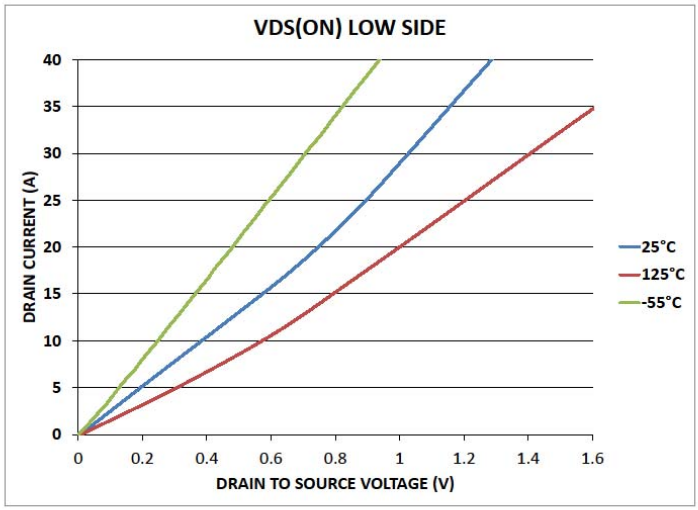
In addition to the externally programmable current limit there is also a fixed internal current limit which senses only the highside current. It is nominally set to 140% of the continuous rated output current. Should either of the outputs be shorted to ground the highside current limit will latch off the output transistors. It will be necessary to remove the fault condition and recycle power to +VCC to restart the circuit.

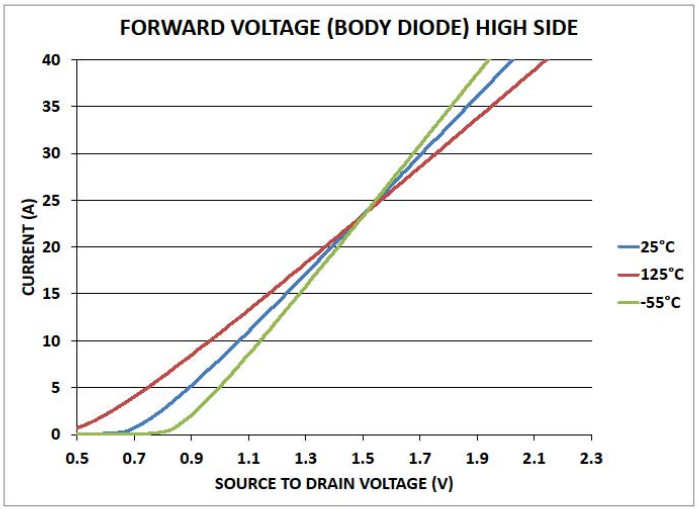
TYPICAL APPLICATION CIRCUIT

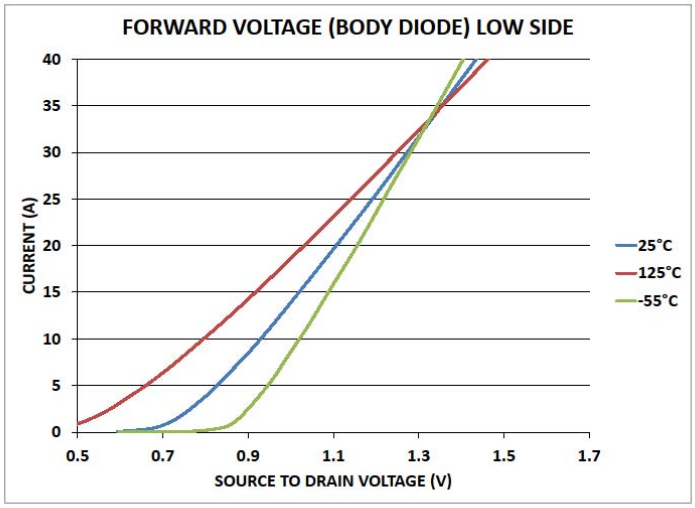


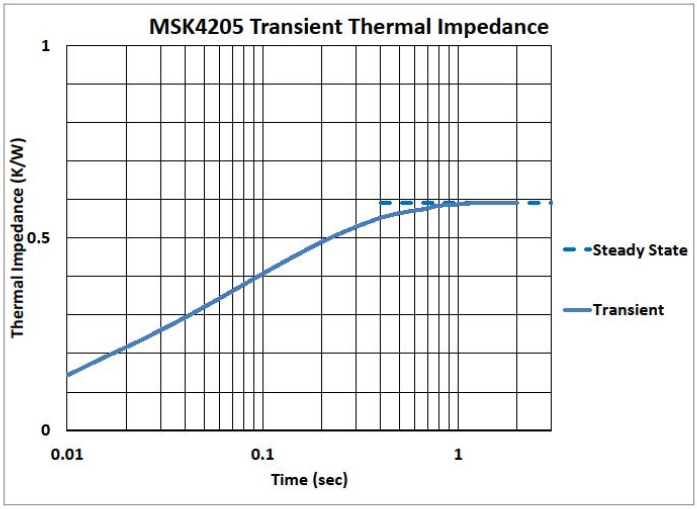
TYPICAL PERFORMANCE CURVES



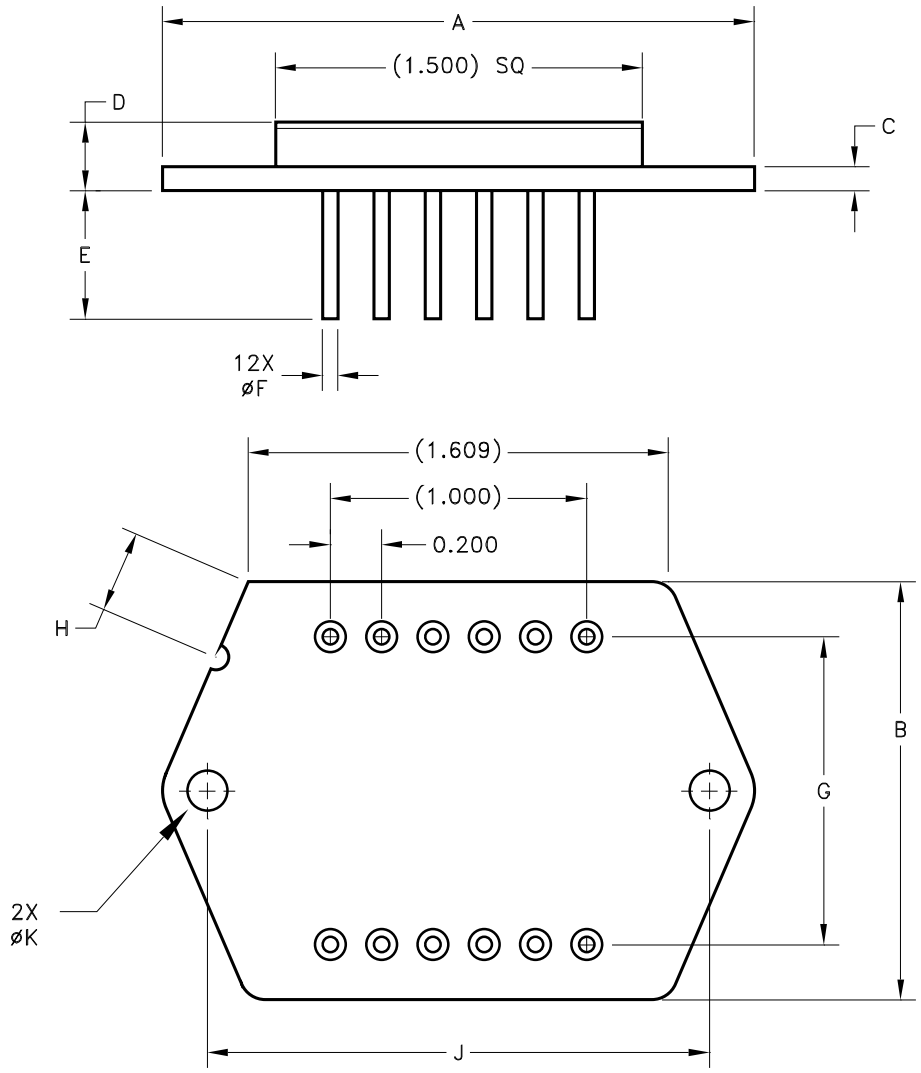








MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	2.299	2.319
B	1.620	1.640
C	0.088	0.098
D	———	0.285
E	0.450	0.500
F	0.058	0.062
G	1.195	1.205
H	0.310	0.330
J	1.954	1.964
K	0.154	0.158

TORQUE SPEC: 8-10 IN-LBS
WEIGHT = 58 GRAMS TYPICAL

ALL DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

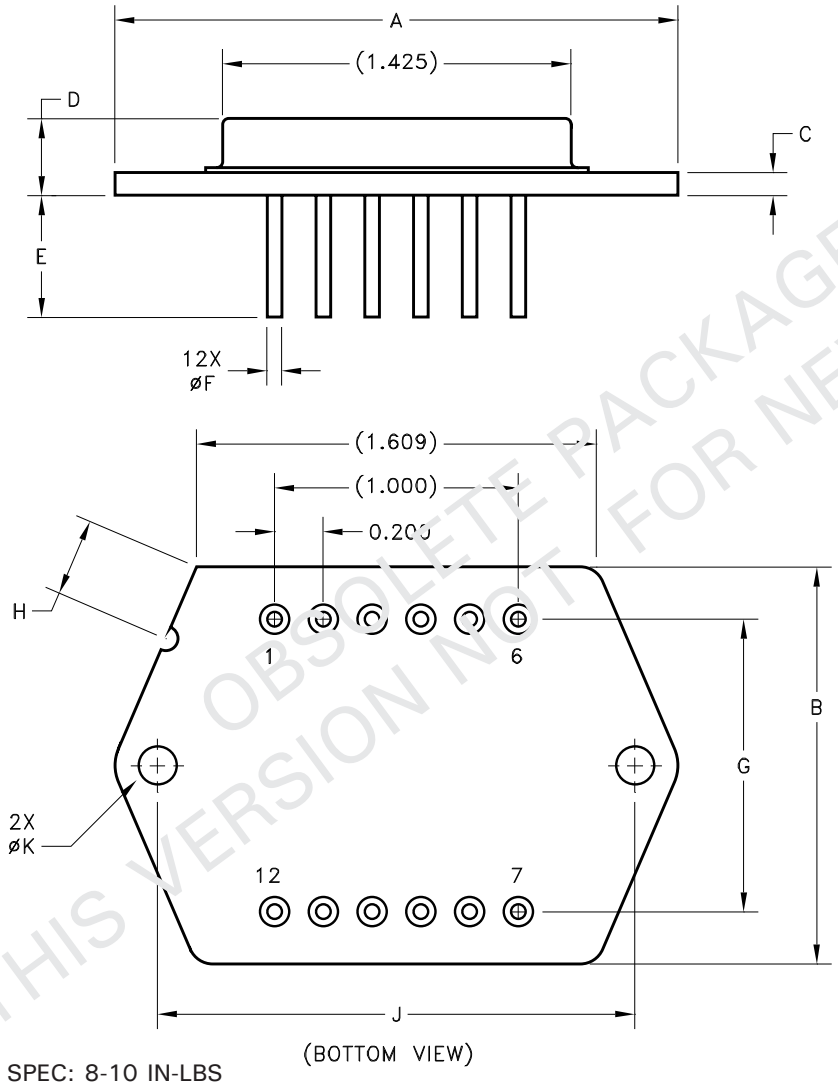
MSK4205H

SCREENING
BLANK = INDUSTRIAL; H = MIL-PRF-38534 CLASS H

GENERAL PART NUMBER

The above example is a MIL-PRF-38534 Class H screened device.

MECHANICAL SPECIFICATIONS



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H	0.310	0.330
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K	0.154	0.158

TORQUE SPEC: 8-10 IN-LBS
WEIGHT = 54 GRAMS TYPICAL

ALL DIMENSIONS ARE SPECIFIED IN INCHES

REVISION HISTORY

REV	STATUS	DATE	DESCRIPTION
G	Released	02/14	Remove T reference, Add weight of tub package.
H	21104	06/14	Add performance curves and update typical body diode forward voltage.

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