TTM Technologies
Time-To-Market Interconnect Solutions™

Global Front-End Engineering Design Package Guidelines

OVERVIEW

The purpose of the legacy Viasystems Design Package Guidelines is to provide direction and clarity to our customers about the necessary contents of data packages for the preproduction engineering and manufacturing of printed circuit boards.

README FILE

Preferred Format: ASCII
Acceptable Formats: Word, Excel, PDF

The Readme file should include the following elements.

- Contact name(s), email address(es), and 24 x 7 contact phone number(s)
- Each part number and its revision history
- A list of all supplied files, including associated file formats
- Information on the merging of image files, if required
- Intentional short/open information (actual nets)

DRILL INFORMATION

Preferred Format: ODB++, EXCELLON II
Acceptable Formats: RS274X, RS274D, Trudril

Drill information should include the following elements or considerations:

- Tool codes and X-Y coordinates
- Finished diameter and tolerance for each hole/slot size:
  Example 1: 0.139" +/- 0.003" (139 mil +/- 3 mil) Example 2: 0.135" – 0.142" (135 mil – 142 mil)
- Quantities for each hole/slot size
- Definitions of holes/slots, i.e., plated or non-plated, via, or press fit
- Drill data alignment with design data. Note: Ensure that you have applied the same X-Y coordinate format, e.g., 2.4, 2.5, as used with the image files.
- The following should be designated and separated into their own drill files:
  - o Filled vias
  - o Blind drills
  - o Buried drills
  - o Microvias
  - o Back drills (filled)
  - o Back drills (non-filled)

DESIGN DATA

Preferred Format: ODB++, Gerber RS274X
Acceptable Formats: Gerber RS274D

Design data should include the following elements or considerations:

- All inner and outer (copper) layers
- All solder mask (SM) layers:
  - o SM features that match the diameter of the outer layer pads
  - o All tented or partially covered pads designated as fill or cap locations
  - o Notification of SM-defined pads
- All legend (silkscreen) layers
- All merged image files (which also should be referenced in the Readme file)
- For the RS274D format, you must provide a single table clearly describing each aperture's shape, dimensions, and Gerber D-code. You must clearly and completely describe the format of each custom nonstandard aperture, including:
  - o Coordinate format, e.g., 2.4, 2.5
  - o Coordinate mode (absolute or incremental)
  - o Zero suppression (leading, trailing, or none)

Design Package Guidelines

- A 1:1 profile of the single image
- Title block included in each PCB layer
- All pads “flashed” with standard aperture shapes, rather than drawn with lines
- All solid copper areas should be designed as a contour or surface area, as opposed to those drawn.
- An overlap of 0.0005” (0.5 mil) for drawn features
- PWR and GND files should not extend beyond the edge of the board by more than by 0.025” (25 mil).
- Use a separate D-code/aperture for multiple impedance circuitry on the same layer: Example: 0.0041”/0.0042” (4.1/4.2 mil) lines
- Do not use a cross-hatch for thieving/CU distribution, as it creates excessive cleanup of silver residue.
- Do not use an output coordinate format of resolution lower than the CAD design settings as it creates registration and edge design irregularities on drawn features.
- Drill output format should match design output format to ensure accuracy of the design. Example: A PCB design with drill output @ coordinate format of 2.6 and design output @ coordinate format of 2.3 should be flagged for correction.

NETLIST

Preferred Format: IPC-D-356, IPC-D-356 A
Acceptable Formats: Mentor Neutral

The supplied netlist data should include the following elements or considerations:

- legacy Viasystems recommends providing a netlist file that is CAD-generated for all design packages.
- Any and all planned shorts or opens in the design must be stated in a fabrication drawing and/or Readme file.

FABRICATION DRAWING

Preferred Format: HPGL/HPGL2, RS274X
Acceptable Formats: Adobe PDF

The fabrication drawing should include the following elements or considerations:

- PCB outline dimensions, including cutouts, chamfers, radii, bevels, and scoring.
- Fiducial locations, slots, and tabs for breakaway rails.
- An X-Y dimension from at least one drilled reference, non-plated hole internal to the board edge.
- A hole chart with symbols and the finished hole quantity, sizes, and tolerances.
- A board via structure, including microvias, blind/buried vias (BBV), and filled and plated-over-through vias.
- Back-drill requirements, including, but not necessarily limited to,
  - o Depth
  - o Must-cut layer/Must-not-cut layer
  - o Hole quantity
  - o Hole size
  - o Top/Bottom drilling
- A finished copper thickness or starting foil weight for each external layer.
- A desired surface finish.
- Define if the finished board thickness is over metal or over solder mask.
- If an array or sub-panel is required, legacy Viasystems recommends providing a separate drawing.
- Define the design specification on the drawing. Note: The drawing should always include an updated revision history.
- The drawing must clearly and fully describe each part profile using standard dimensioning and tolerancing practices.

LAYER STACKUP

Preferred Format: HPGL/HPGL2, RS274X
Acceptable Formats: Adobe PDF

The layer stackup should include the following elements or considerations:

- A finished board thickness and tolerance, i.e., surface finish specification
- Controlled impedance requirements (if applicable), including limitations on
  - o Trace width, i.e., the 85 Ohm differential must apply to a minimum 0.0055” (5.5 mil) line.
  - o Tolerance, i.e., +/- 10%: For each requirement, you must list its impedance layer and each associated reference layer.

Design Package Guidelines

- Material requirements, including either the specific material name, i.e., supplier name, such as Isola FR408, or the details necessary to select a material, including the
  - o RoHS[1]/peak assembly temperature
  - o Df/Dk requirements for a certain frequency
  - o IPC-4101 slash sheet
  - o Lead-free assembly requirements
- Copper (CU) weights for all integrated circuits.
- A finished CU thickness, or starting foil weight, for each external layer
- Define if the finished board thickness is over CU or over solder mask.
- Define if each layer is **signal** or **plane**, including whether plane layers are designated **PWR** (Power) or **GND** (Ground) and the voltage levels that PWR layers are operating at.
- Additional specific requirements, such as
  - o Layers that must use two-ply dielectrics
  - o Minimum or maximum thickness for specific dielectric layers
  - o Specific glass styles
  - o Line width/pitch constraints
- Impedance routing constraints, such as a differential pair of traces that must be routed between pads or antipads of a certain diameter on a certain pitch

THERMAL MANAGEMENT (TM) DESIGNS (COINS AND/OR PALLETS ATTACHED)

3-D Model

Preferred Format: 3-D STEP Solid Model: Settings AP203, Advanced B-Rep
Acceptable Formats: CADKEY Design File (CKD)

The **3D model of a TM design** should include the following elements:

- Both a 3-D model and design drawing for all machined parts
- Drawing of specific features for all machined parts such as coins and pallets
- 3-D model of the PCB associated with the coin or pallet assembled part. **Note:** This model should illustrate mechanical parts only, not circuitry!
- Drawing of specific features for the assembled PCB and any associated coins and pallets. **Note:** This drawing should illustrate only the board with its attached coins and/or pallets, not the top-level assembly!

TM DRAWING

Preferred Format: CADKEY Design File (CKD)
Acceptable Formats: AutoCAD Drawing (DXF), Adobe Acrobat (PDF)

The TM drawing for a TM Design should include the same appropriate items as those for 3-D Model above.

ODB++ FORMAT

ODB++ format is the preferred format for Design and Drill data. While it is an excellent format for importing into the CAM application, applying appropriate attributes to the design features has been proven to reduce cycle times, reduce potential quality errors during the tooling process, and eliminate technical holds which impact delivery to the customer.

- **Filled Surfaces** – all solid surfaces should be represented as polygons and not “line filled” surfaces.
  - o Minimal vertices/features equals vastly improved DRC processing time and significantly reduced cleanup time. No cleanup also equals less chance for error.
- **Pad attributes** – Component pads and vias can be defined as vias or toeprints. If they are toeprints, then they are either a SMD (and marked as such) or they are a PTH.
  - o **Customer placed SMD attributes will help assure correct SM modifications for shaves and clearances at SMDs. Also, this saves time by not having to add SMD attributes and assures all SMDs are selected correctly.**

[1] *Restriction of Hazardous Substances Directive*

Design Package Guidelines

- **Teardrop** – all teardrops should be marked with the proper teardrop indicator. This differentiates them from other pads on the design.
  - o Customer placed teardrop attributes will assure the customer gets teardrops where desired and are easily selected if replacement is desired.
- **Impedance Lines** – There already exists in ODB++ a Boolean type attribute that can be used to mark copper whose impedance characteristic is critical to the design. The desired impedance is not included, simply the fact that circuits are impedance related. (There is a definition of .diff_pair and .dpair_gap already in ODB++ version 7 that could also be populated.)
  - o Customer placed impedance attributes assure accurate selection and will allow automation. Impedance attributes will also help the operator determine priority when editing.
- **Copper text nomenclature** – An existing attribute can be used to indicate copper that is part of constructed text.
  - o Customer placed nomenclature attributes on copper layers assures correct selection of text and will also help the operator determine priority when editing.
- **Tie bars** – On designs with fingers it is not uncommon to receive an outer layer with copper shorting all the fingers together. These copper features should have the non-electrical attribute in order to not upset the netlist.
  - o Assure correct netlist reports in Genesis.
- **ICT** –There is an attribute (ICT Test point) for this purpose. The reason is that the copper serves no purpose to bare board manufacturing, but the manufacturer still would like to understand why the copper surface is not covered with Soldermask.
  - o Customer placed ICT test point attributes assure correct selection of test points and allow for automated verification of full clearance at all ICT test point locations. They will also help the operator determine priority when editing.
- **Press-fit component holes** – There are times that knowing a component pin is press-fit versus pth is important to bare board manufacturing. For example, one should never let the low side of the drill tolerance be smaller than the low side of the press-fit pin. Otherwise the press-fit component pin would not fit.
  - o Customer placed press-fit hole attributes assure correct selection and allow for automation for correct hole size selection.
- **Netlist exception** – Create a summary of known netlist opens and shorts.
  - o Assures correct netlist reporting and removes the time needed for communication back to the customer on already customer known issues.
- **Never create R0 features** – It has been reported the r0, s0 and NULL features create issues during software usage. The suggestion is to simply never create them in the first place.
  - o Customer removed non-graphic features save clean-up and DRC processing time and assure correct features are removed.
- **Fiducials** – Fiducials should be marked as such to enable proper manufacturing validation. Components should be marked with expected counts.
  - o Customer placed Fiducial attributes assure correct selection of Fiducials and allows for automation of size, location and count verification.
- **Copper weights** – Within existing ODB++ format there is a defined place of target cu weight in ounces. There is also a place for layer thickness. Layer thickness is used to calculate the aspect ratio by the analysis today.
  - o Customer placed cu weights and layer thickness attributes assure correct selection of cu weight and layer thickness. Allows for automation to set DRC parameters (spacing, sliver, etc.) to desired MFG requirements per cu weight and layer thickness.
- **Via type** – How vias are to be created, drilled, laser or photo is already an attribute and can be added to via holes.
  - o Customer placed via type attributes assure correct selection and allow for automation of checks for annular ring and correct SM clearance modifications.
- **Via treatment** – If a via is to be capped, this is implemented within the format through attributes eliminating the concern for an improperly capped via.
  - o Customer placed via treatment attributes assure correct hole selection and allow for automation of specific customer selected via treatment process.
- **Pattern Fill**
  - o Customer placed thieving or pattern fill assures correct pattern fill keep out, size and location. A .pattern fill attribute allows for automation of design rule checks.
- **Backdrill**
  - o Customer placed back drill files assures correct location, size and depth. A .back drill attribute allows for automation of design rule checks.